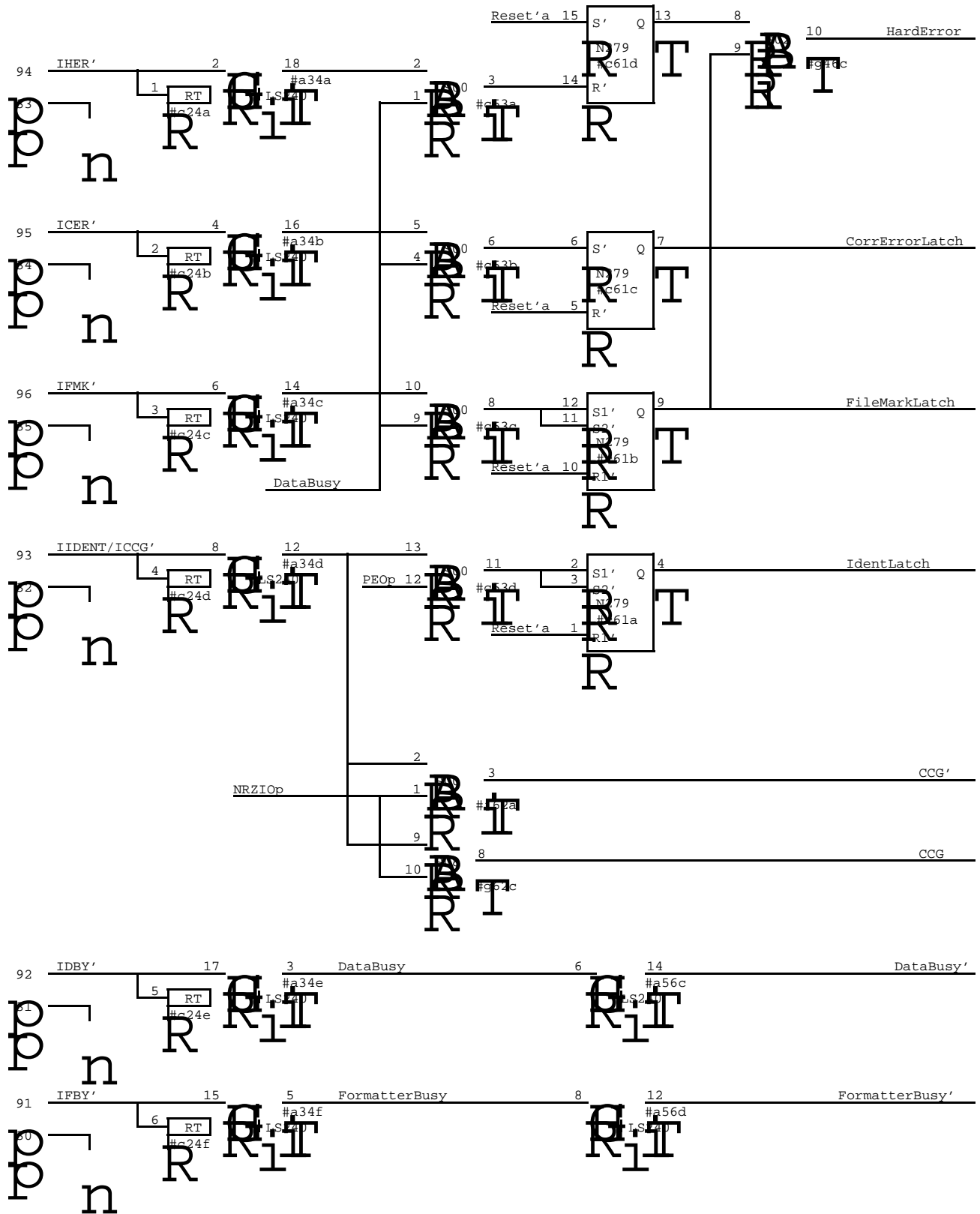
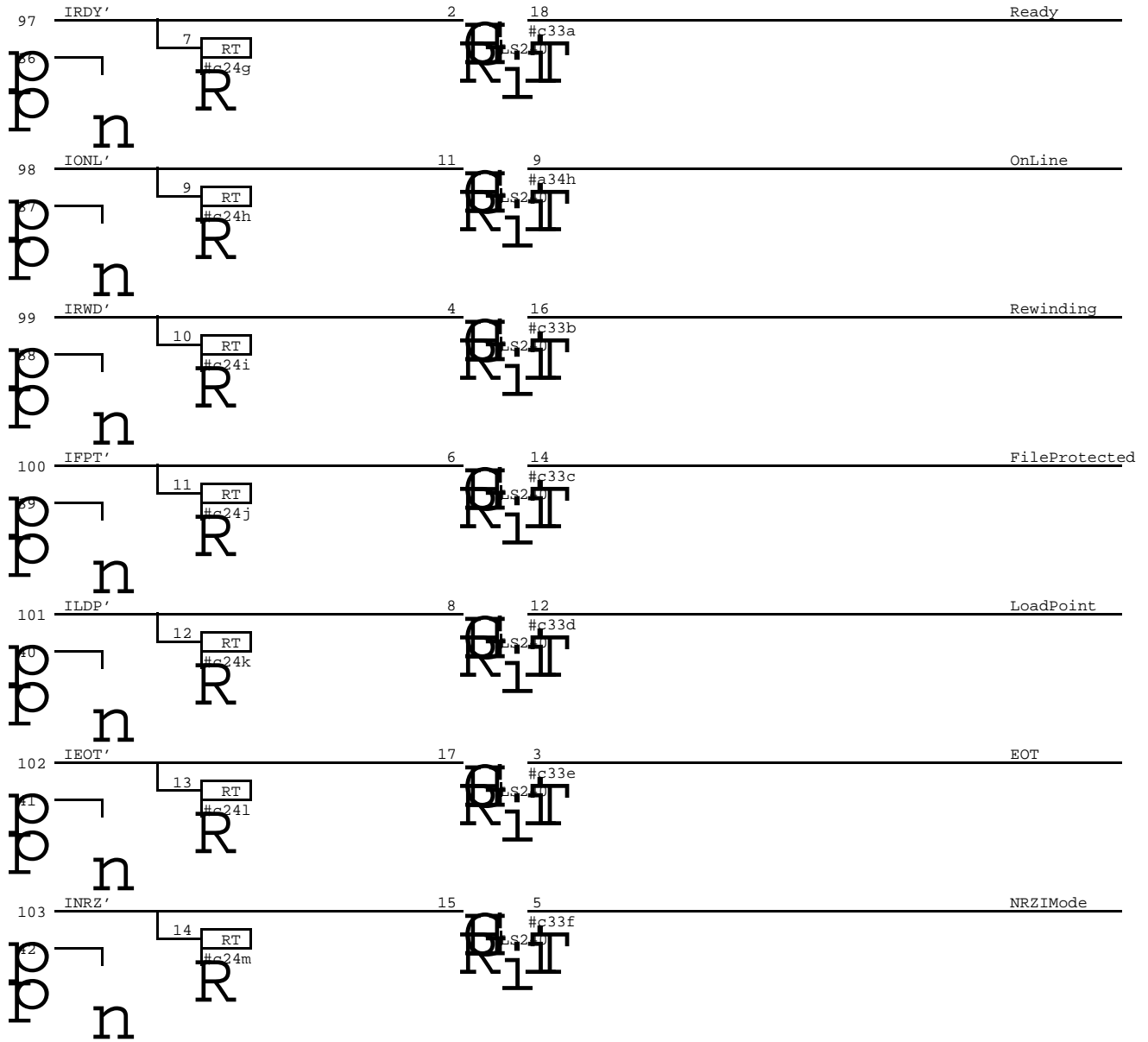


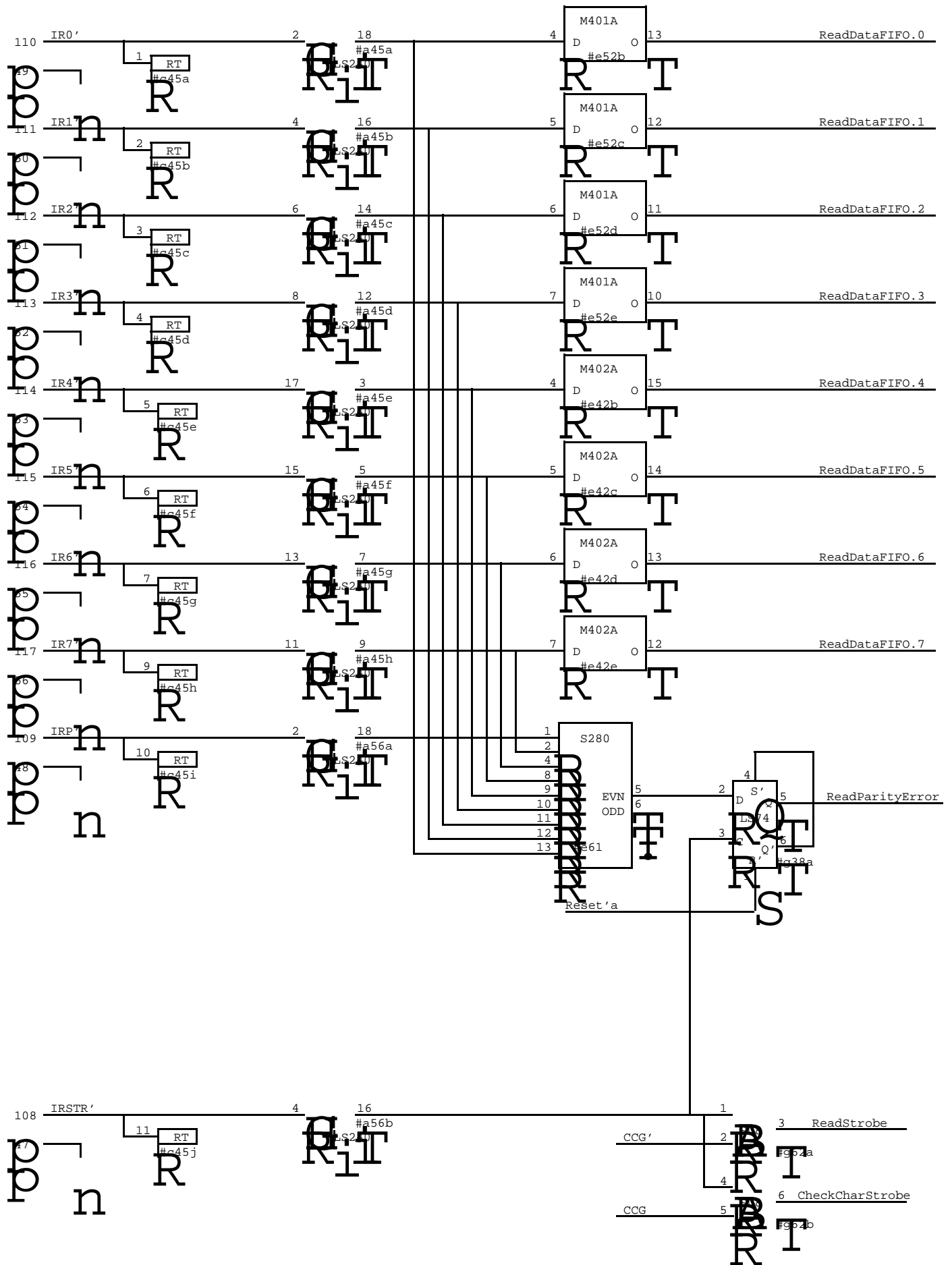
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 T A P E   C O N T R O L L E R  
 D D T a p e

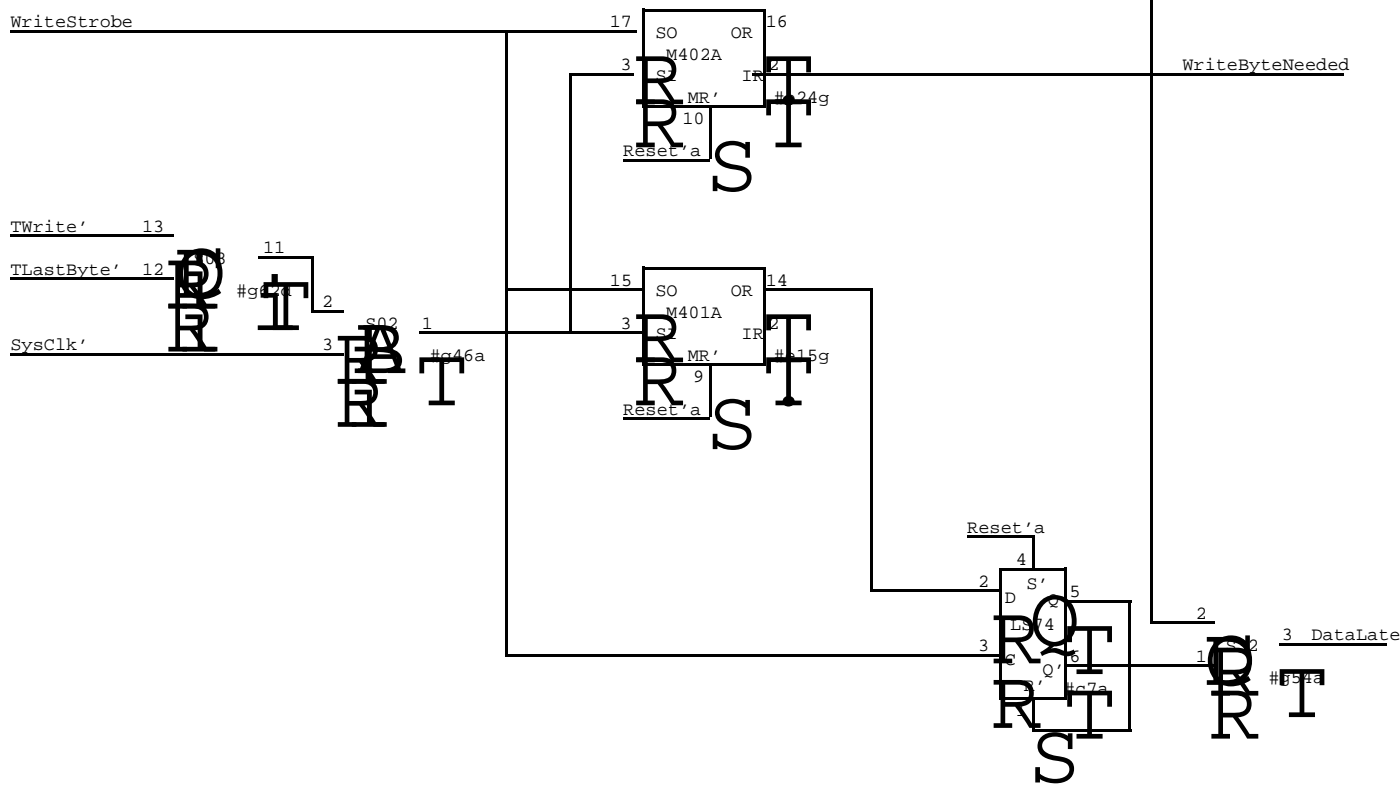
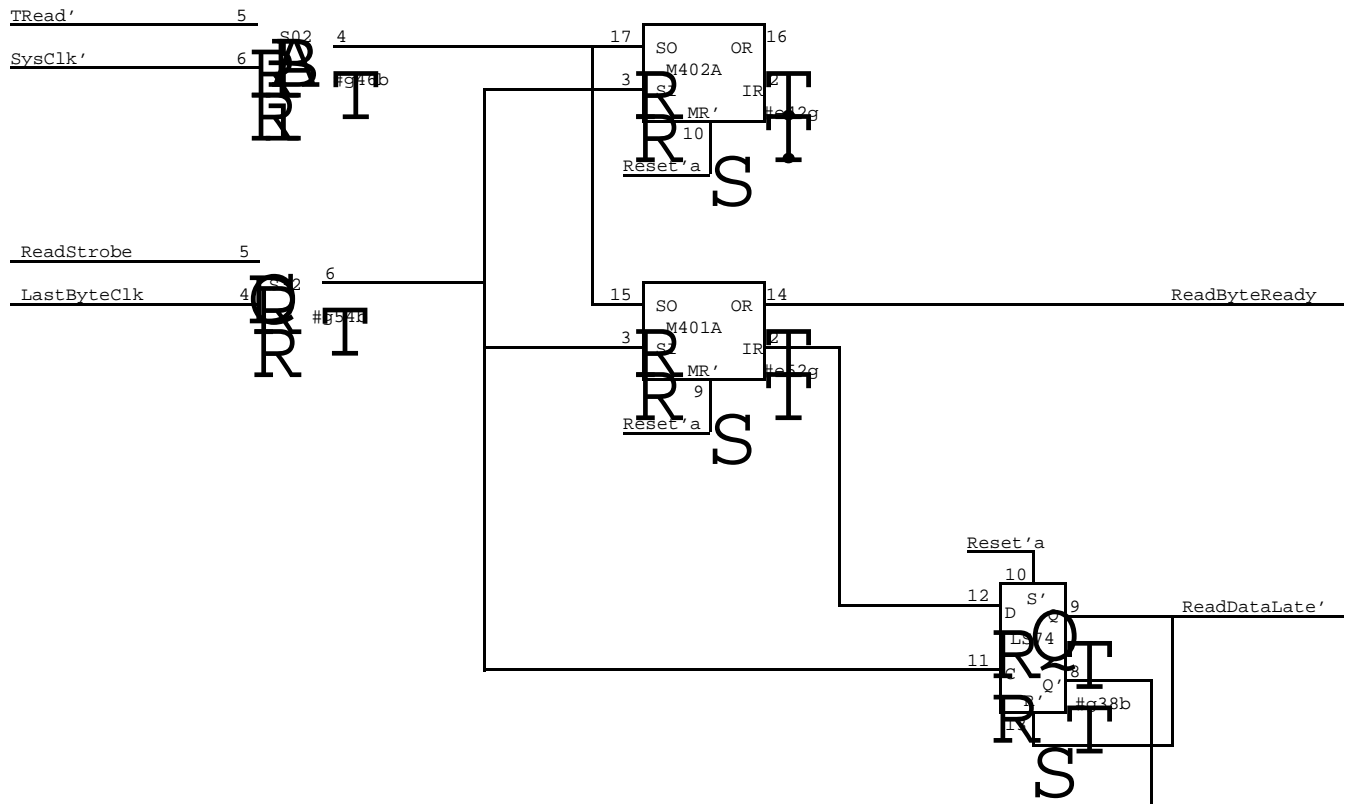
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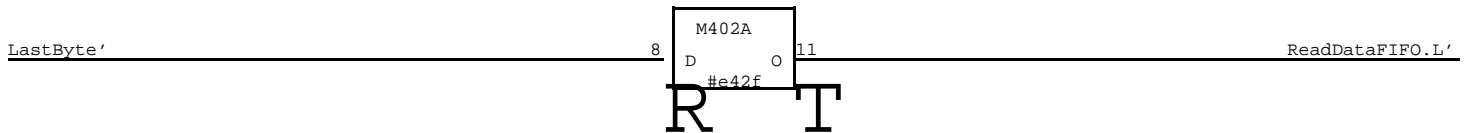
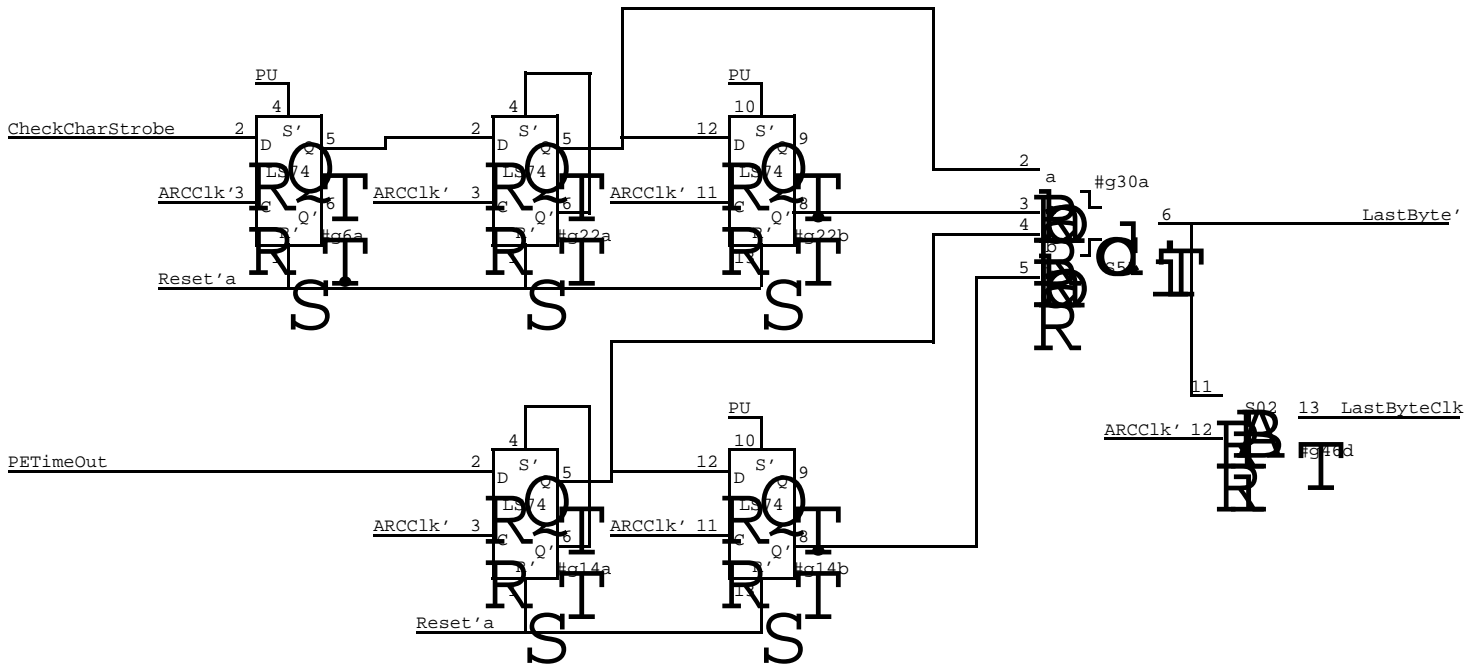
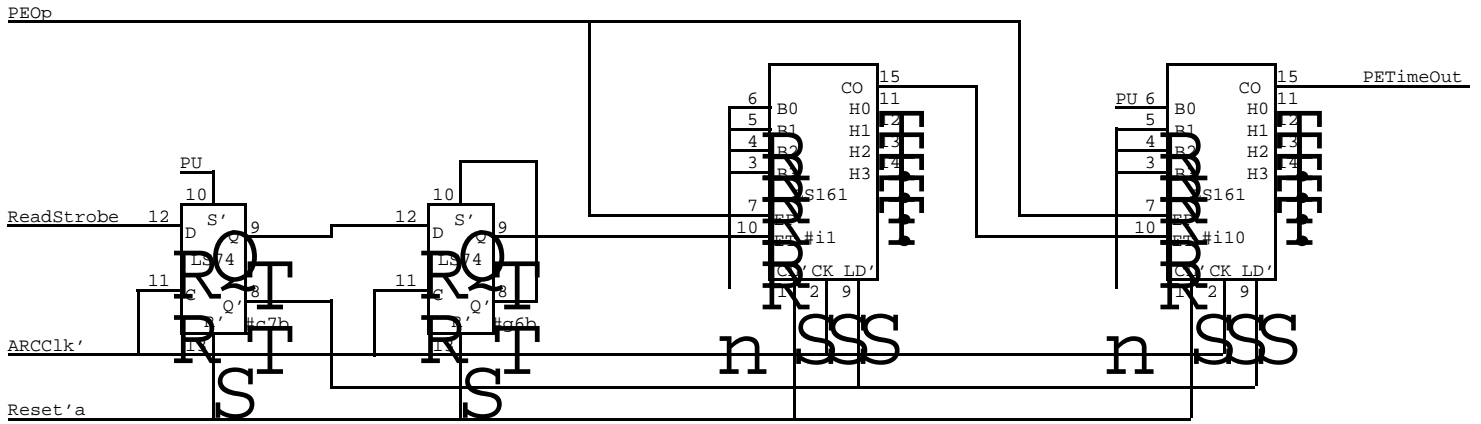
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Formatter Status _____	0 1
Tape Unit Status _____	0 2
Read Data Interface and FIEO _____	0 3
FIFO Control _____	0 4
Last Byte Detect _____	0 5
Write FIFO and Drivers _____	0 6
Formatter Command Register _____	0 7
Go Command Register _____	0 8
Alto Bus Interface _____	0 8
Alto Processor Interface _____	1 0
Data Wakeups _____	1 1
Other Wakeups _____	1 2
Route Stuff _____	1 3
Layout _____	1 4

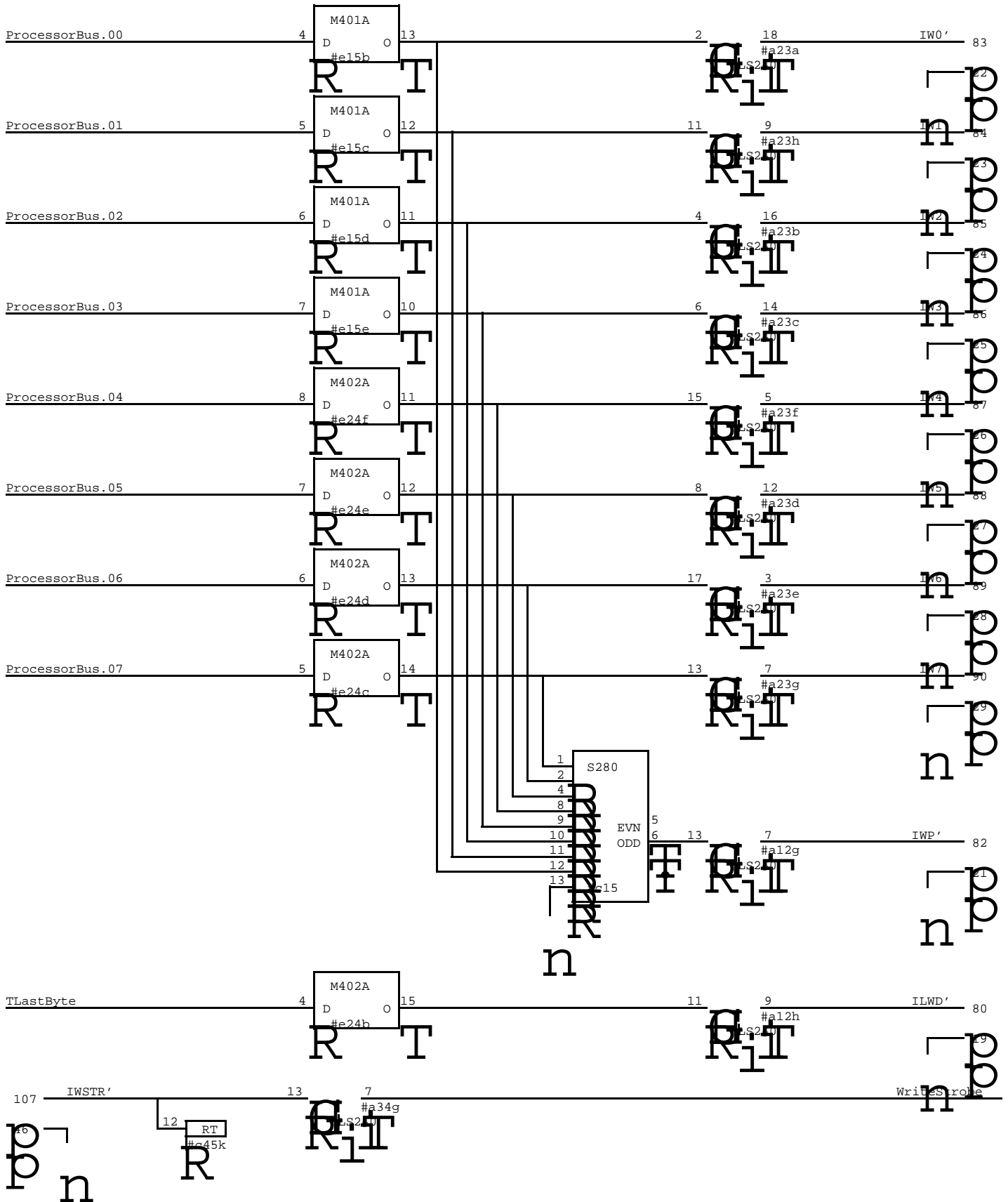


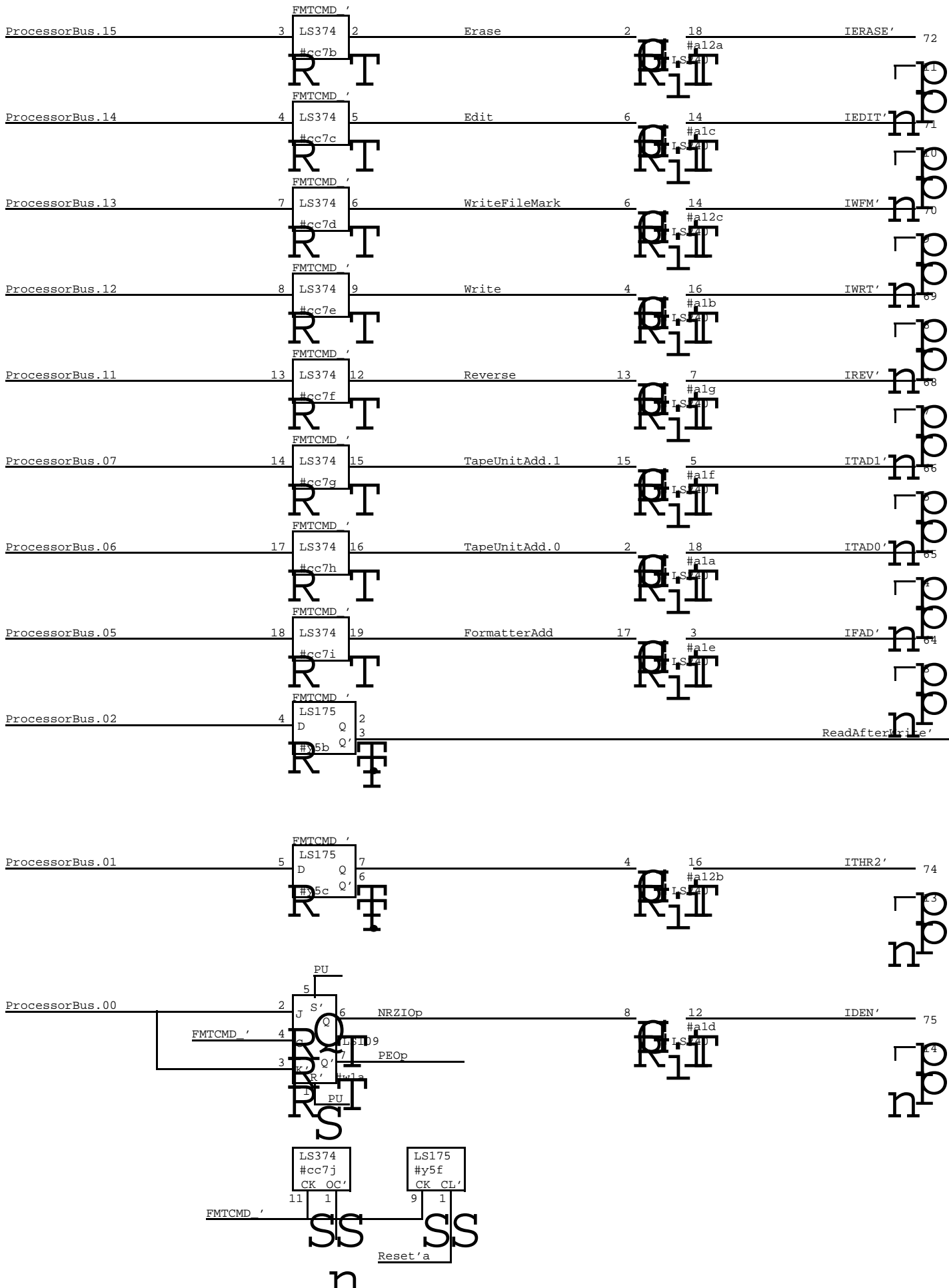




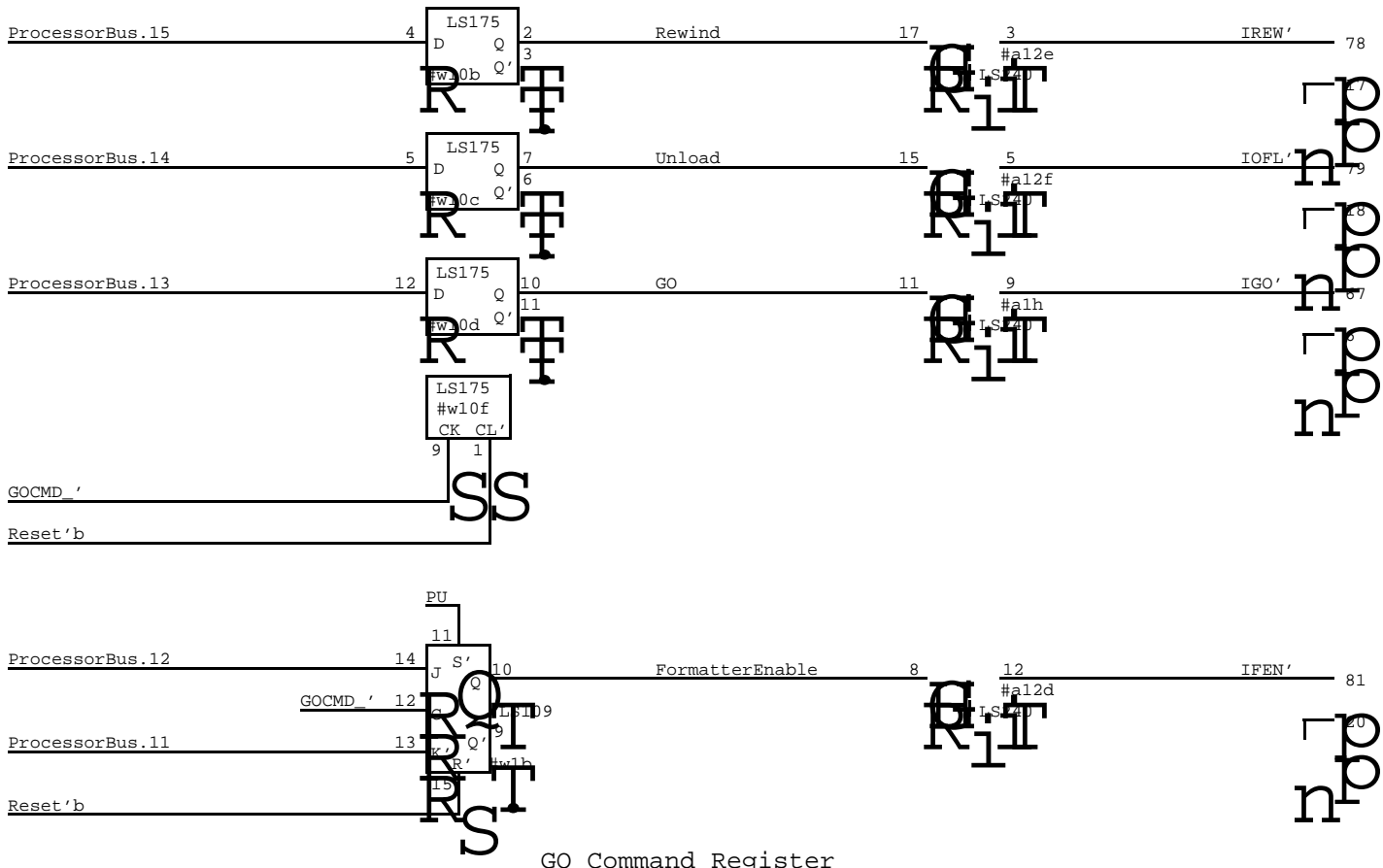




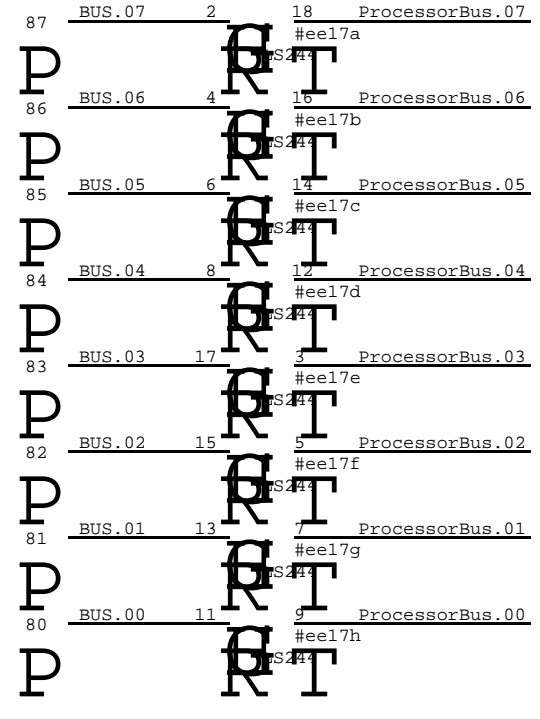
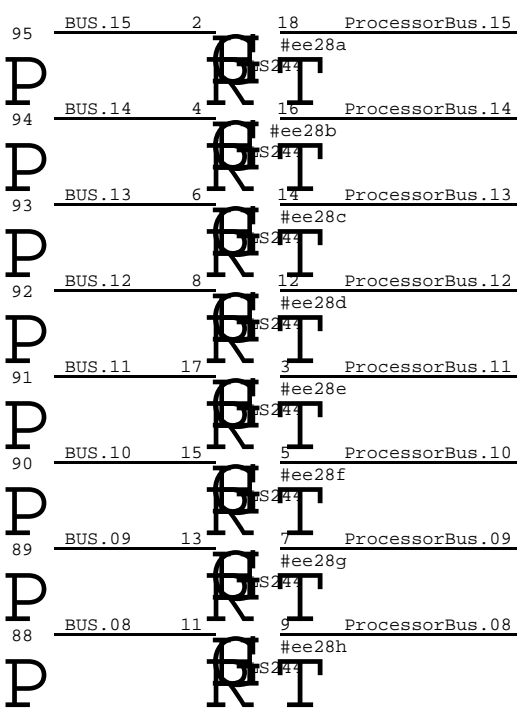






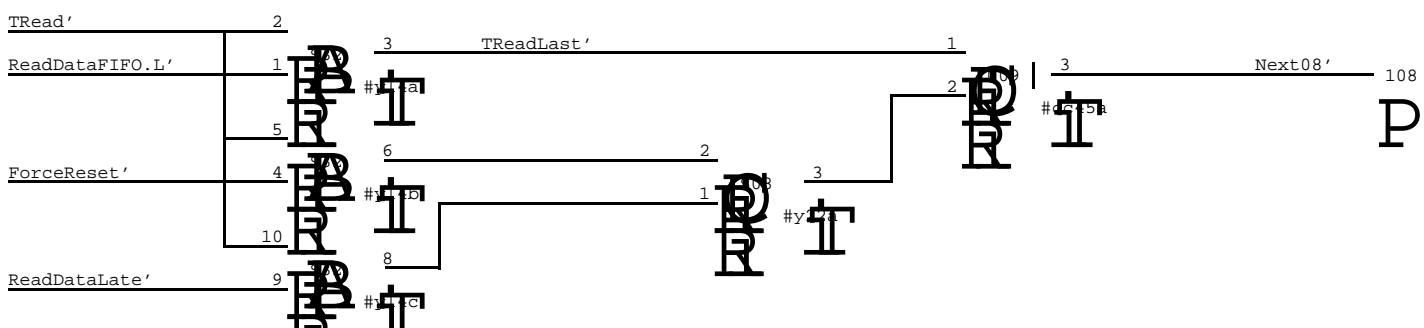
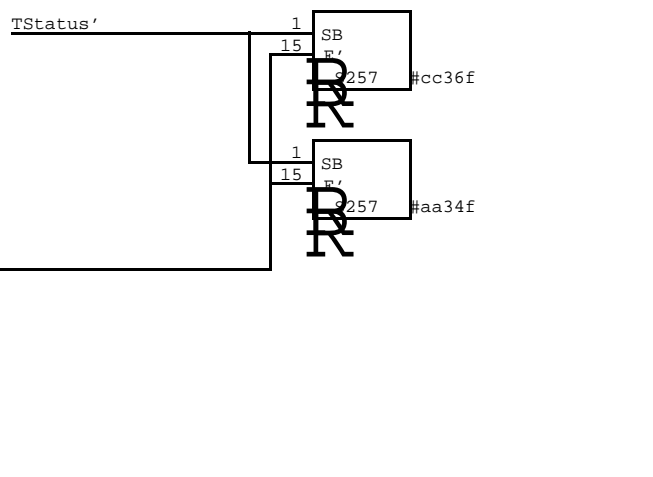
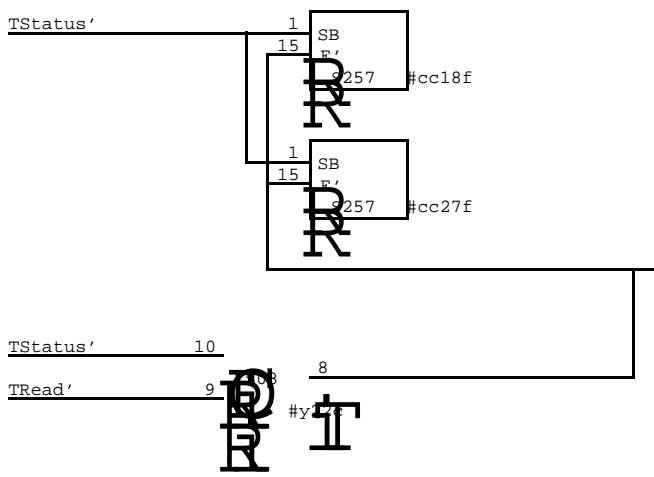
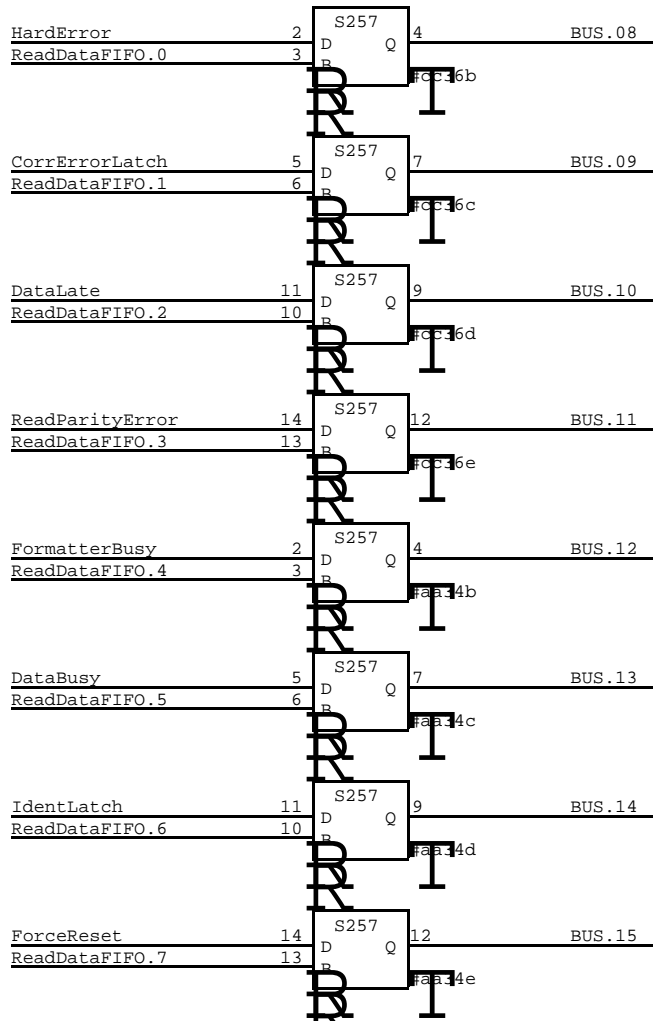
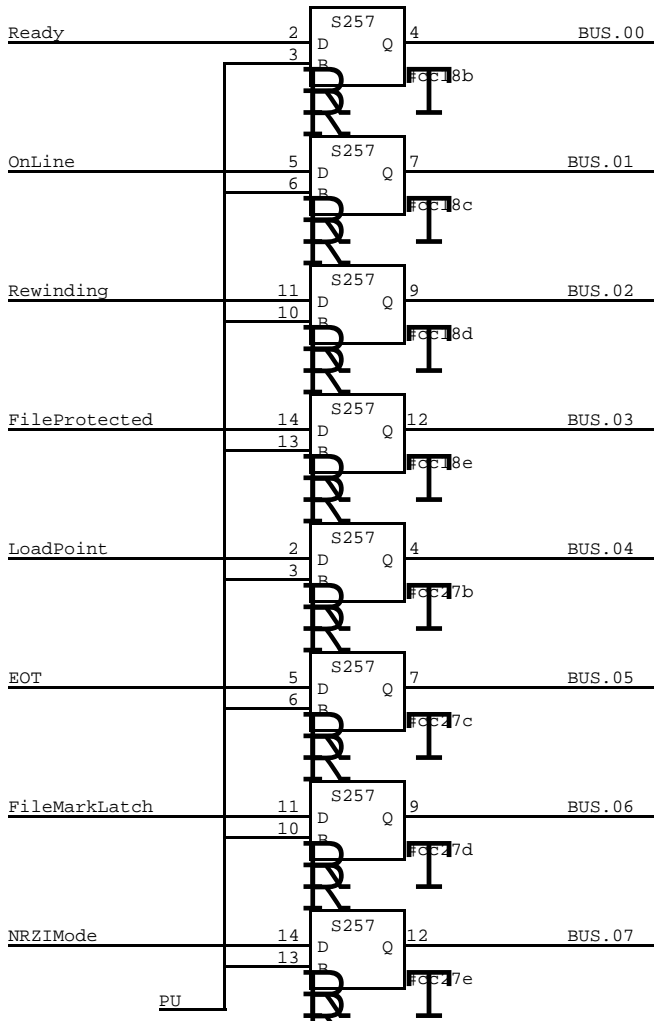


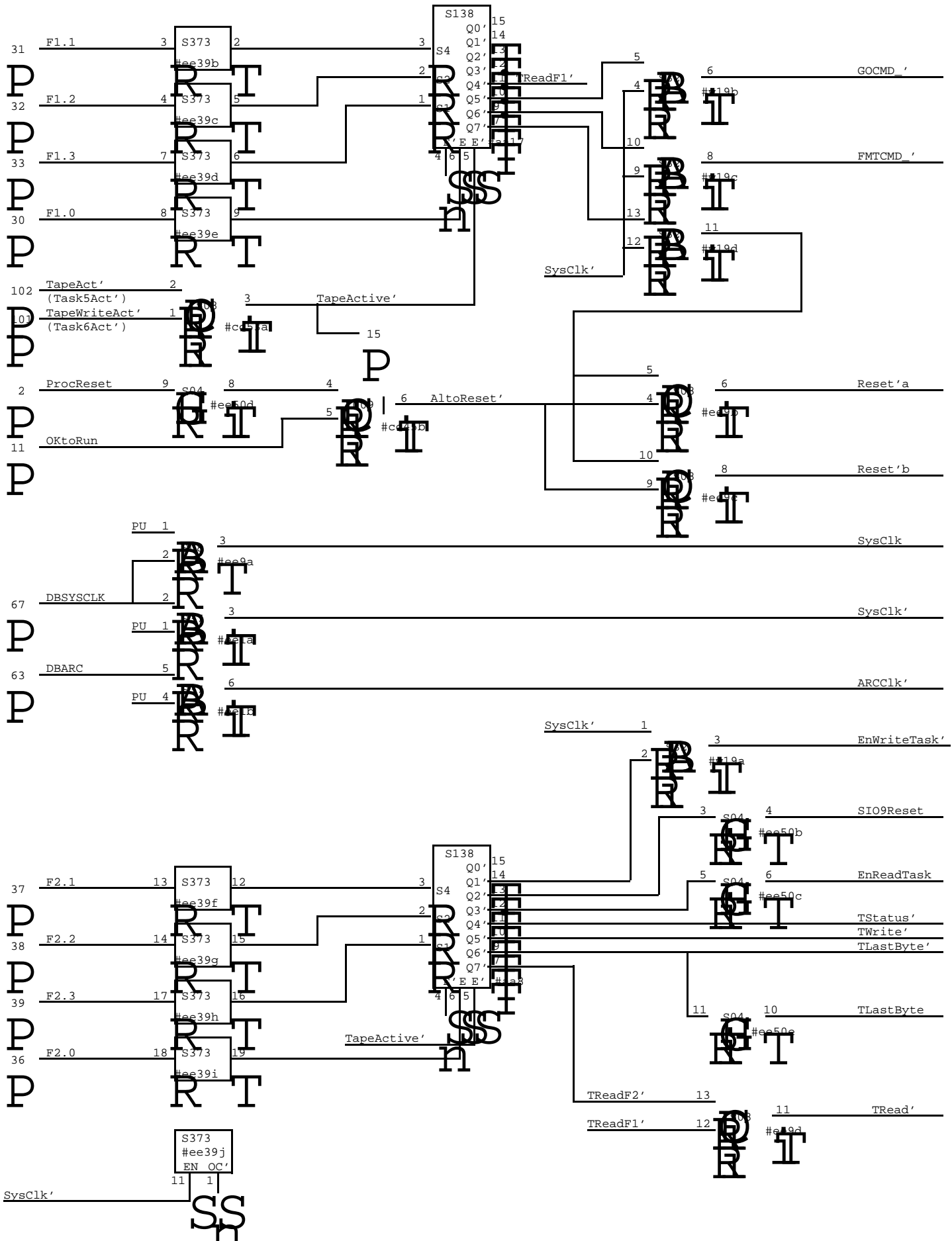
GO Command Register

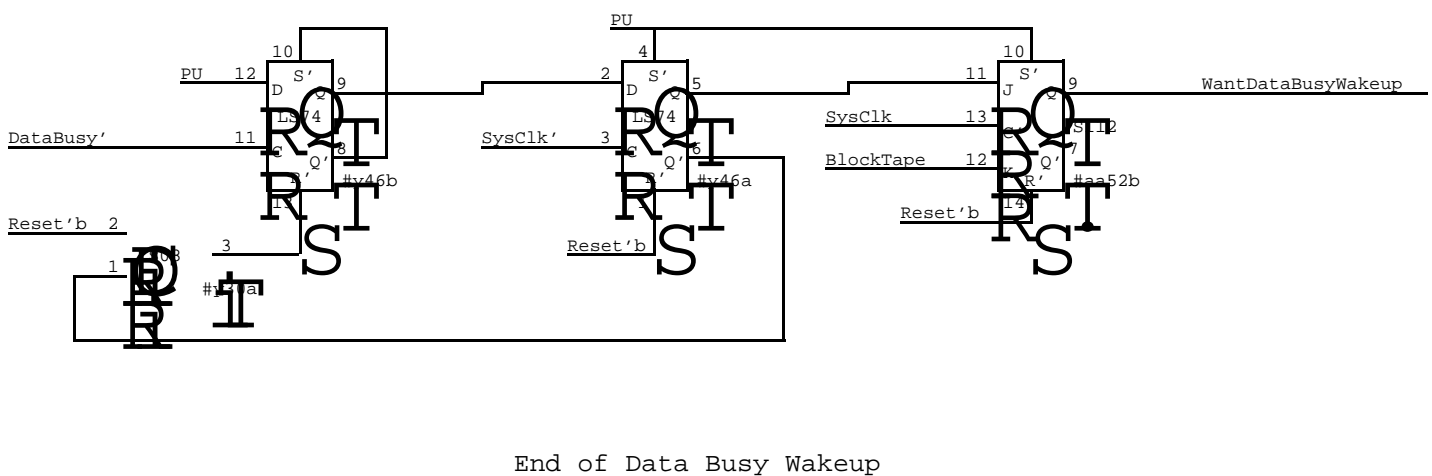
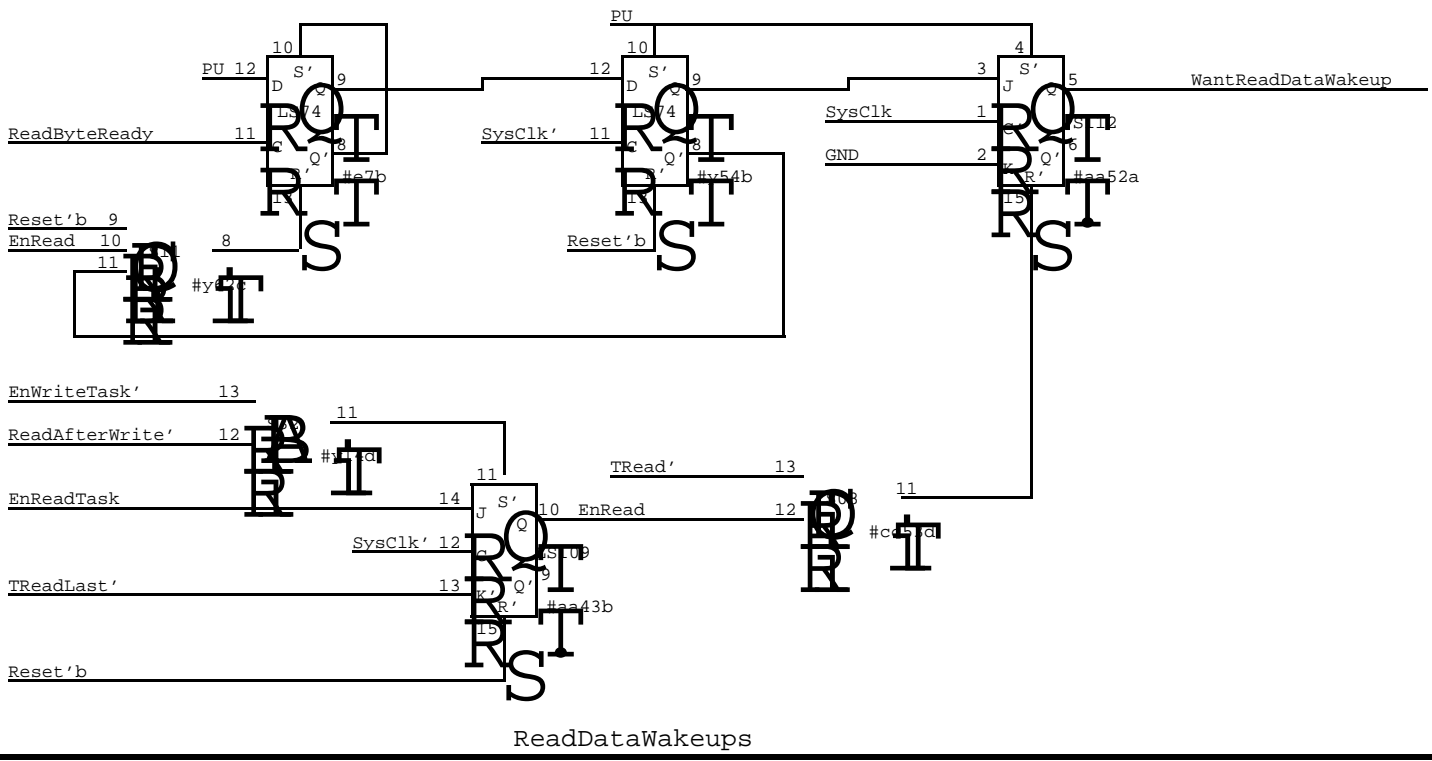
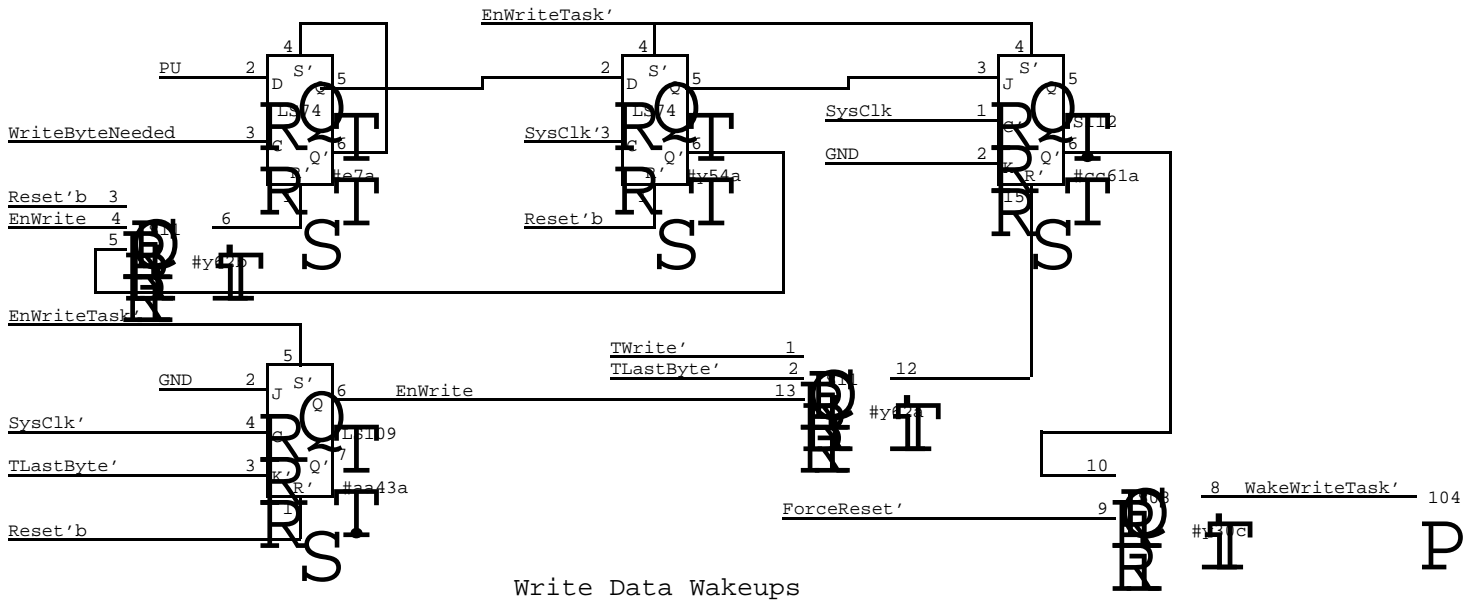


Alto Bus Interface

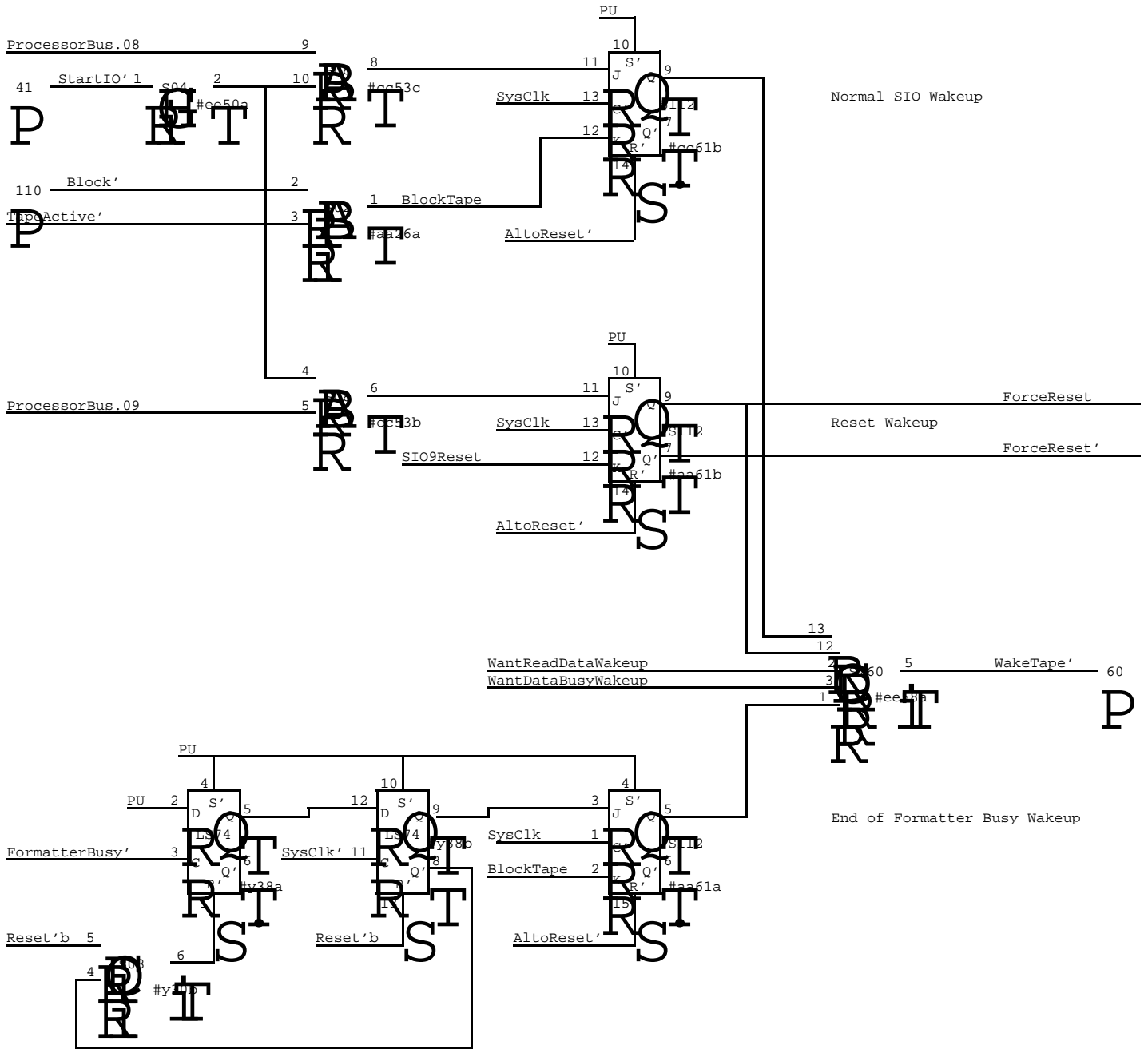
XEROX PARC/CSL	Project DDTape	GO Command Register Alto Bus Interface	File DDTape08.sil	Designer Tim Diebert	Rev B	Date 12/18/80	Page 09
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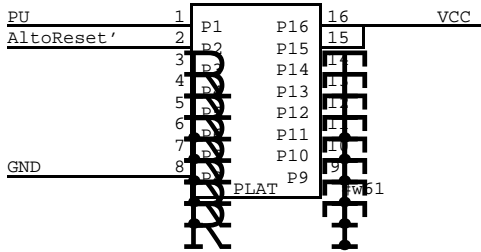
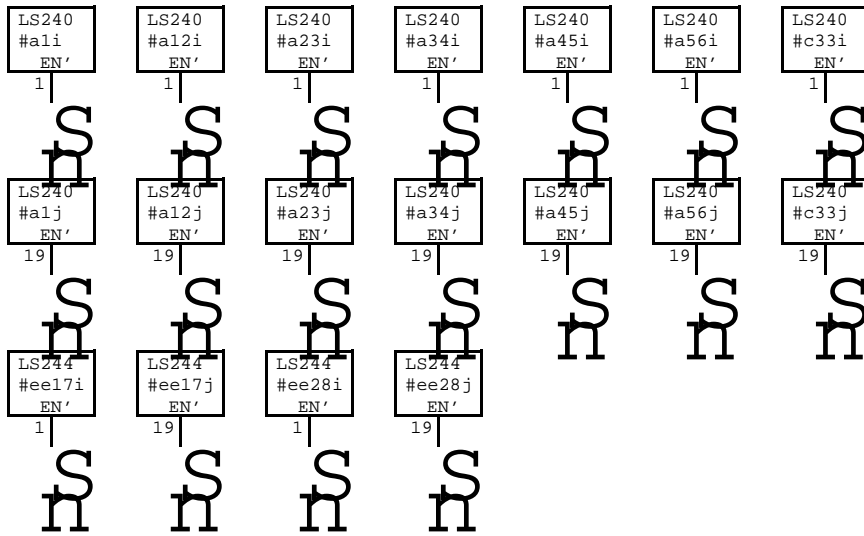






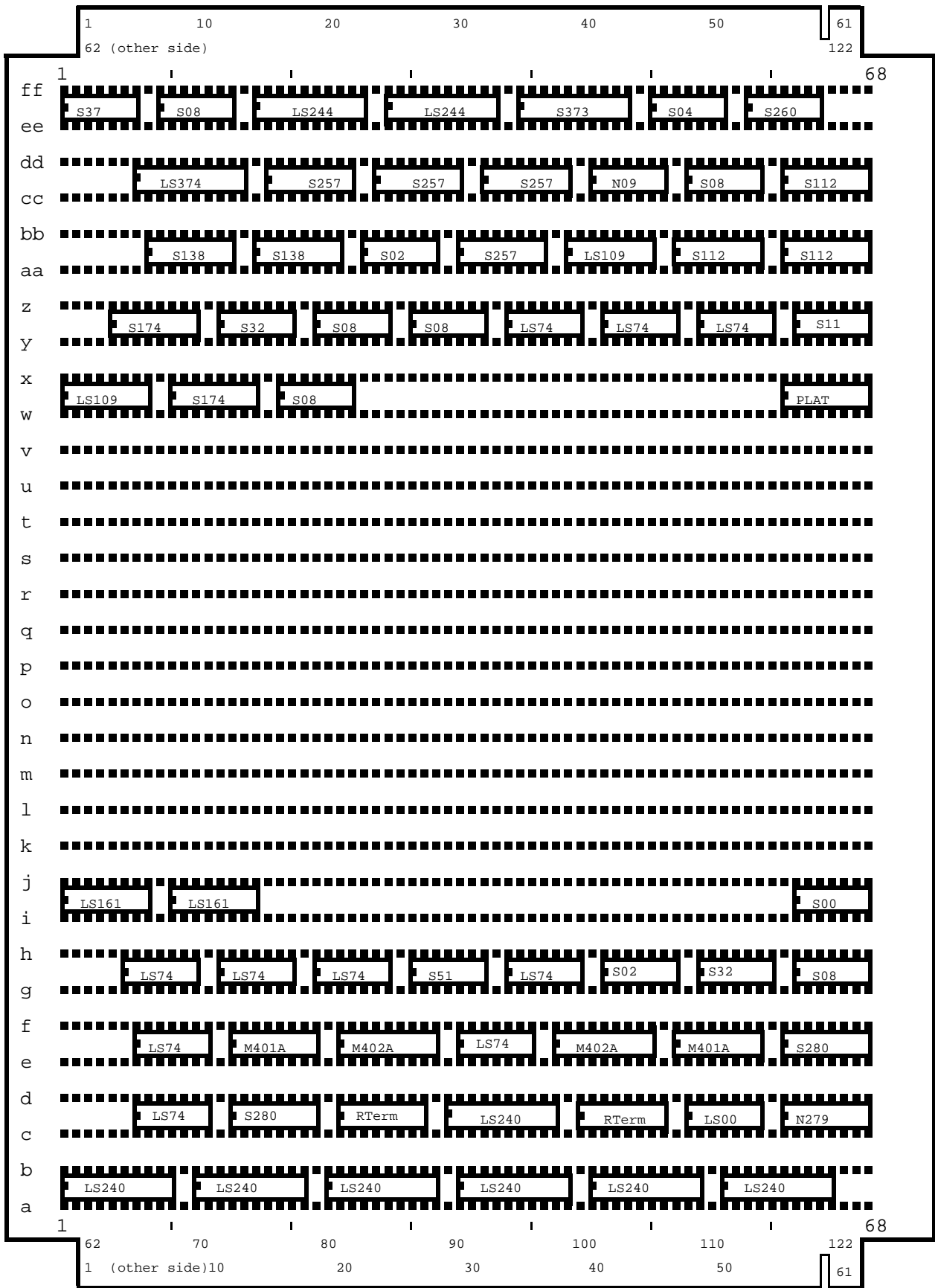
XEROX	Project	File	Designer	Rev	Date	Page
PARC/CSL	DDTape	DDTape11.sil	Tim Diebert	B	12/18/80	12
	Data Wakeups					





1k ohm resistor from 1 to 16  
 330 ohm resistor from 2 to 15

E D G E   C O N N E C T O R



C A B L E   C O N N E C T O R

As viewed from the component side

XEROX PARC/CSL	Project DDTape	Reference Layout	File DDTape14.sil	Designer Tim Diebert	Rev B	Date 1/28/81	Page 15
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