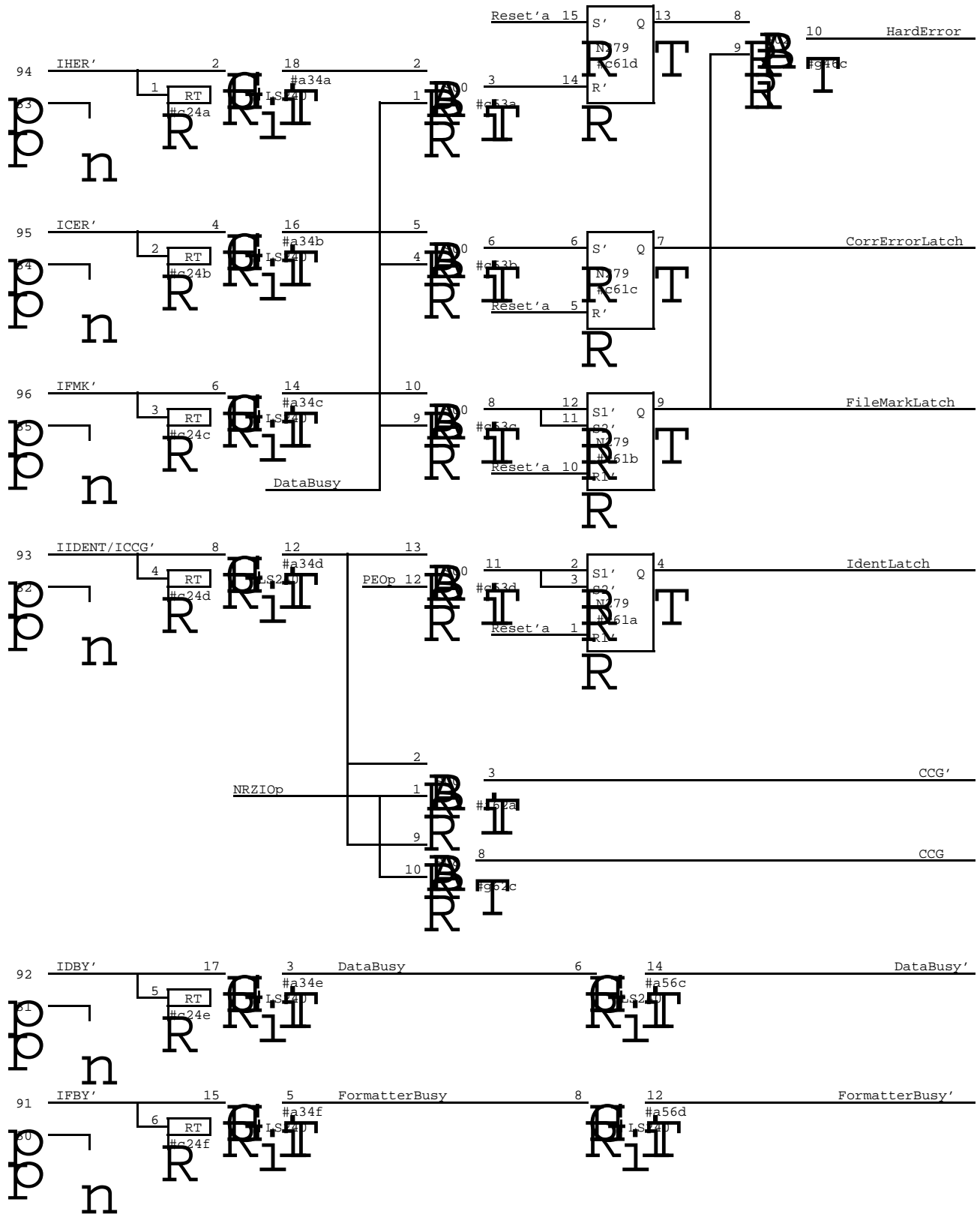
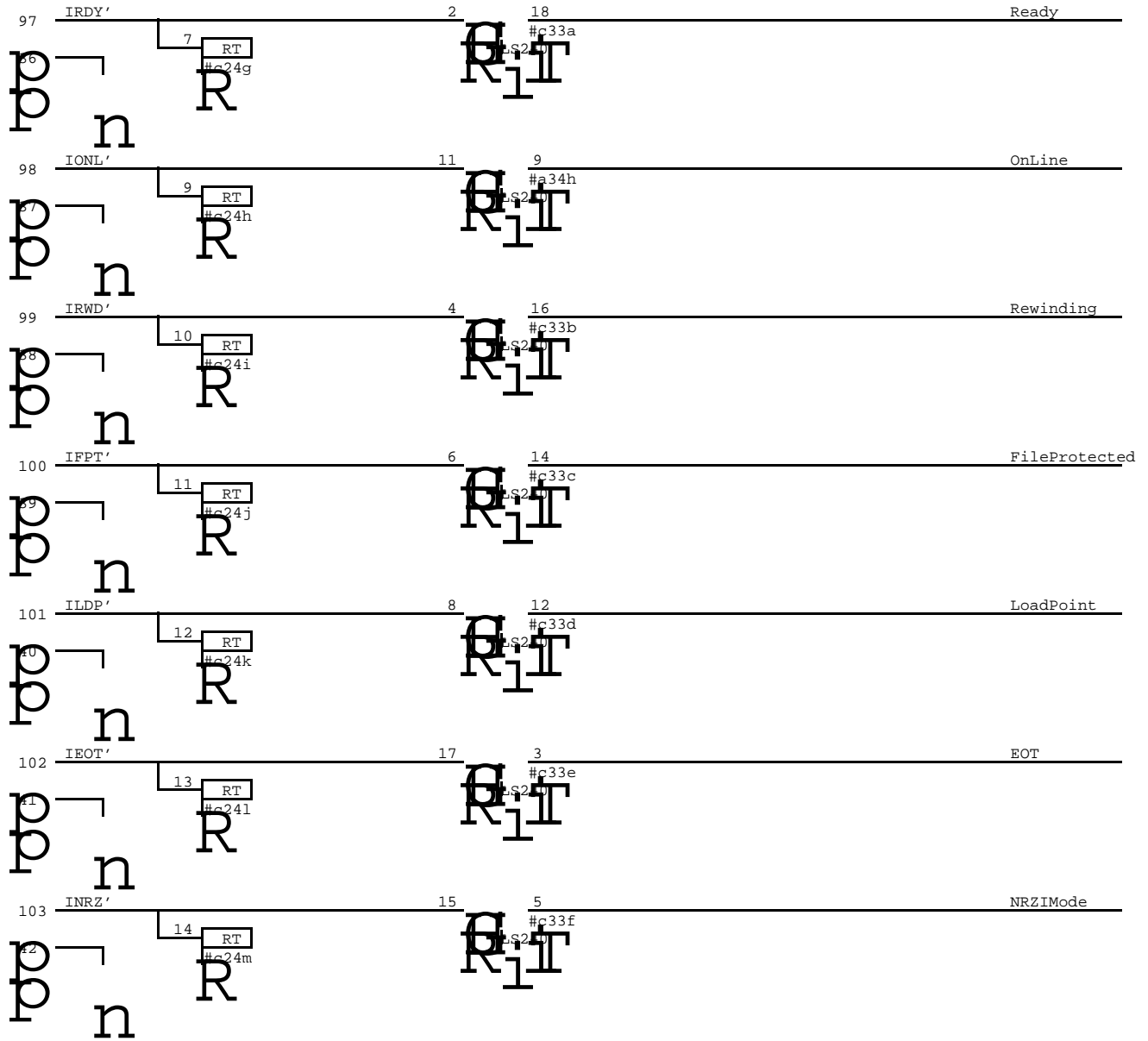


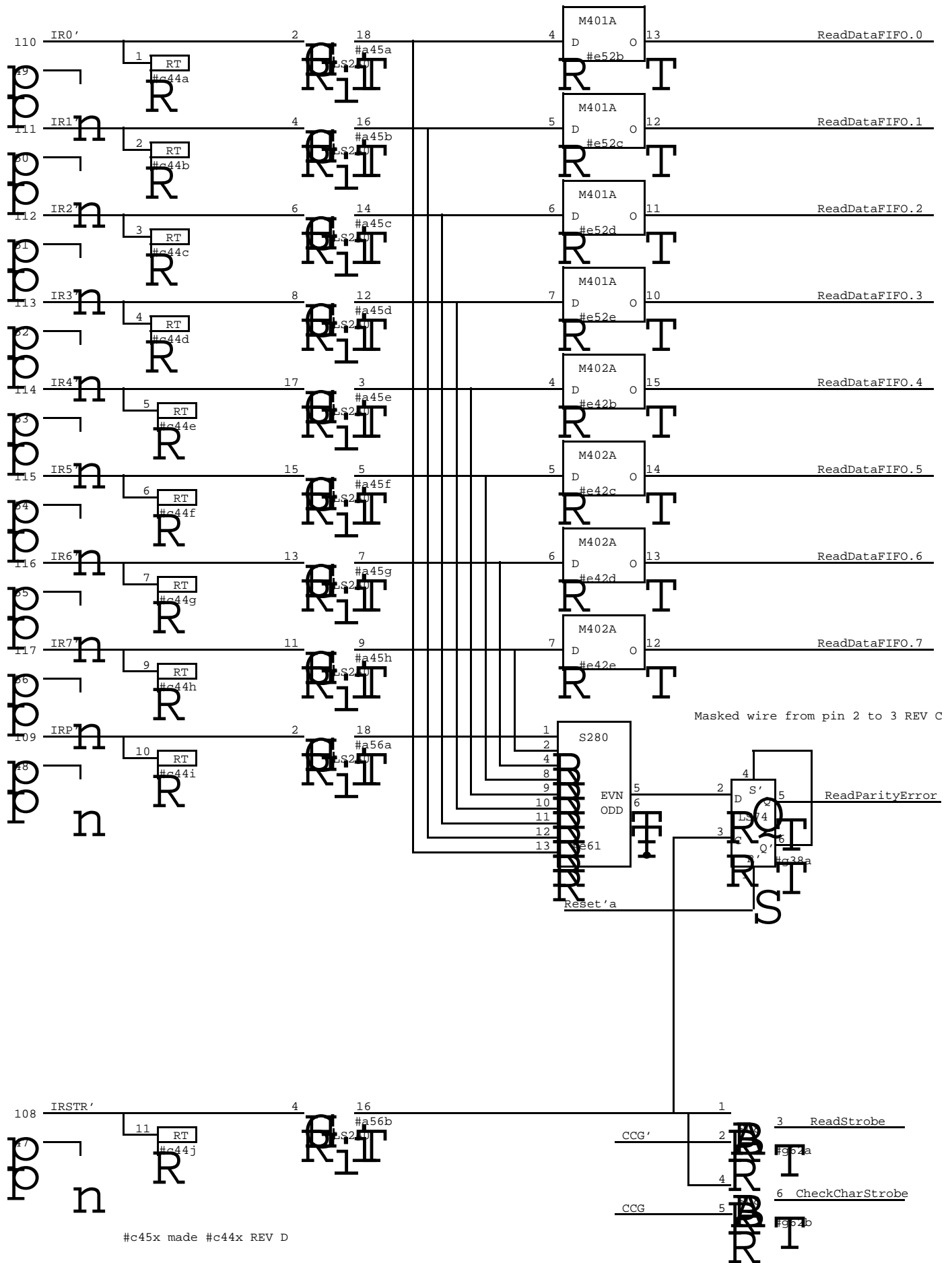
A L T O D U A L D E N S I T Y
 T A P E C O N T R O L L E R
 D D T a p e

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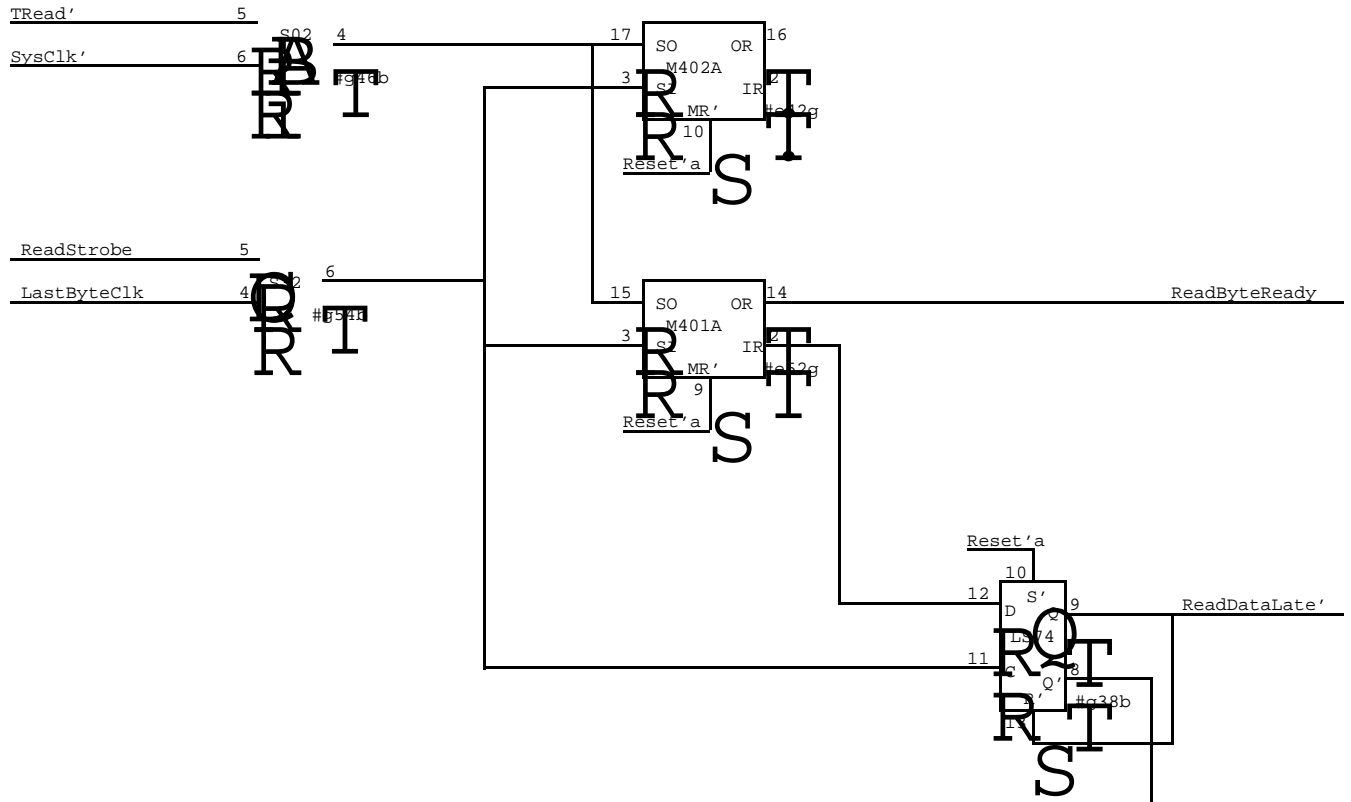
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Formatter Status _____	0 1
Tape Unit Status _____	0 2
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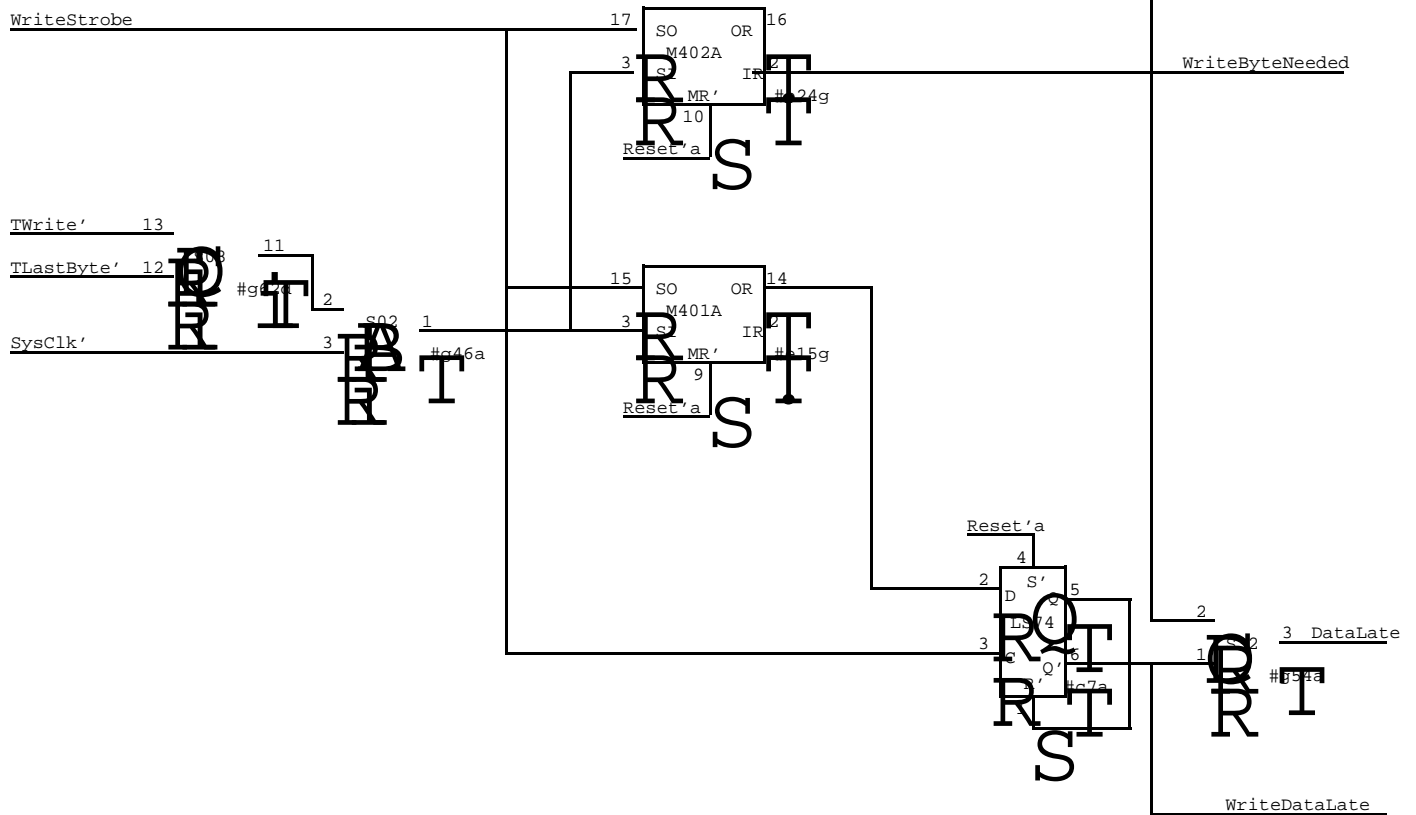




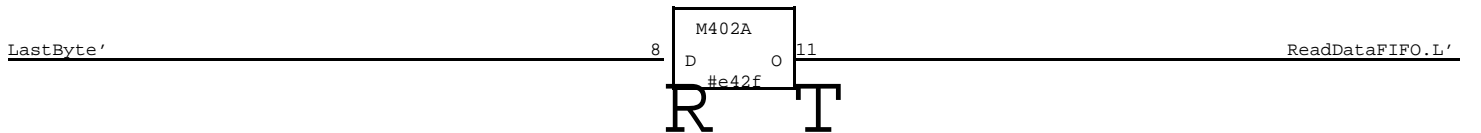
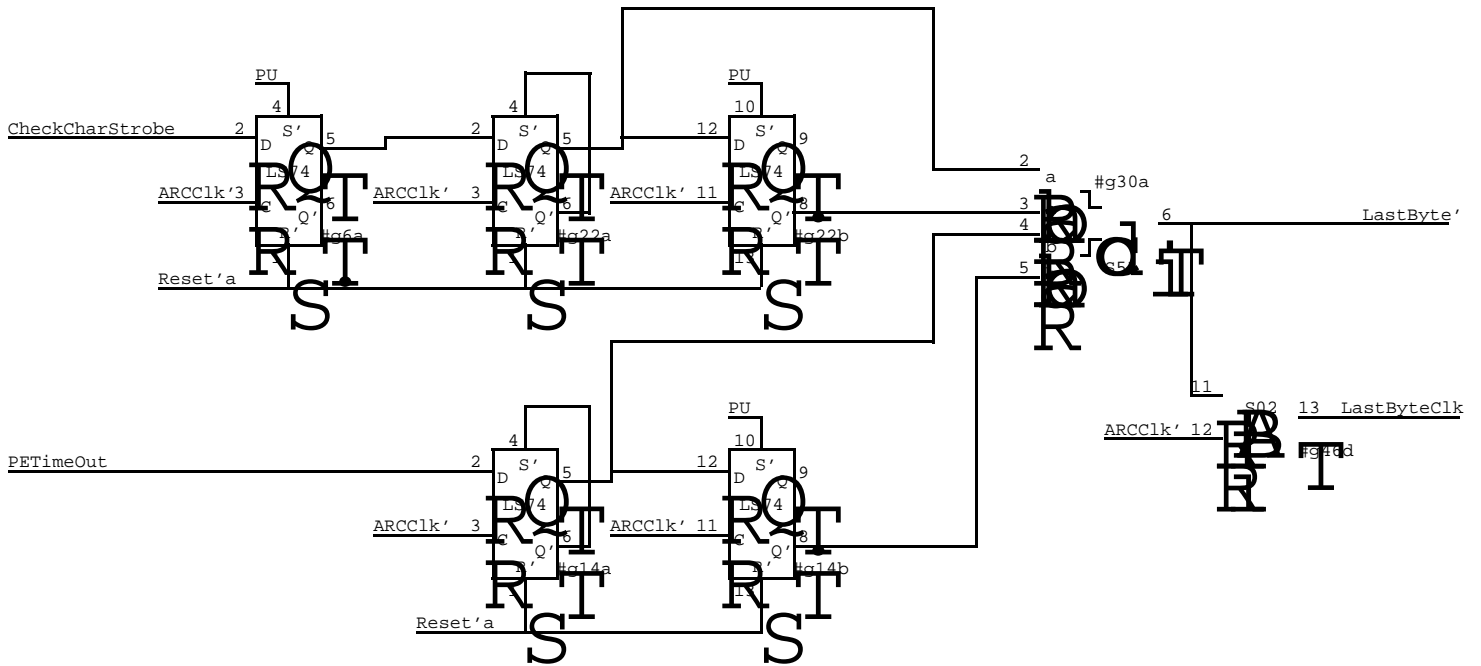
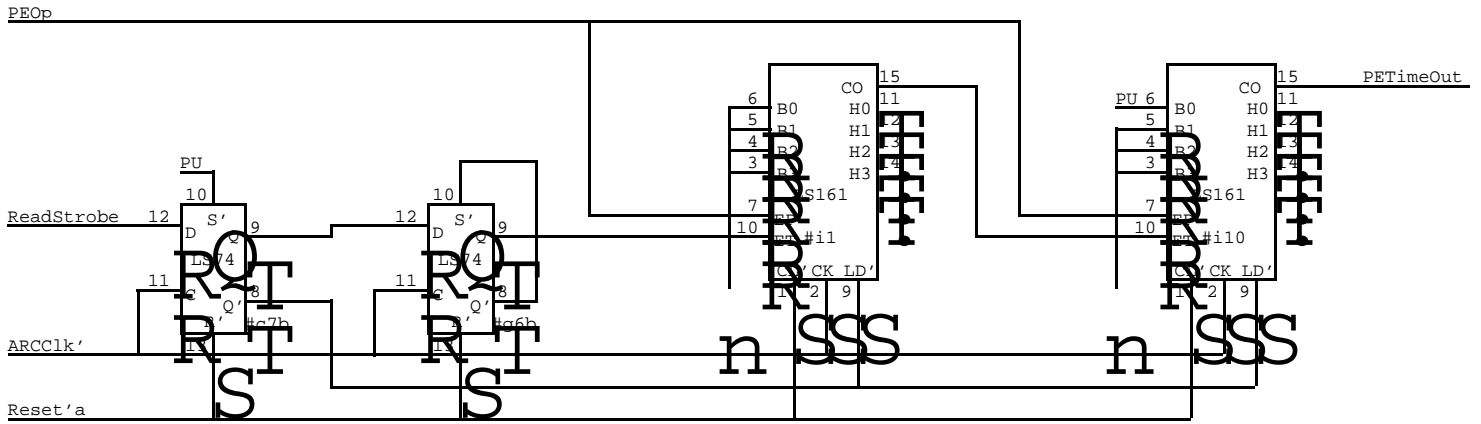
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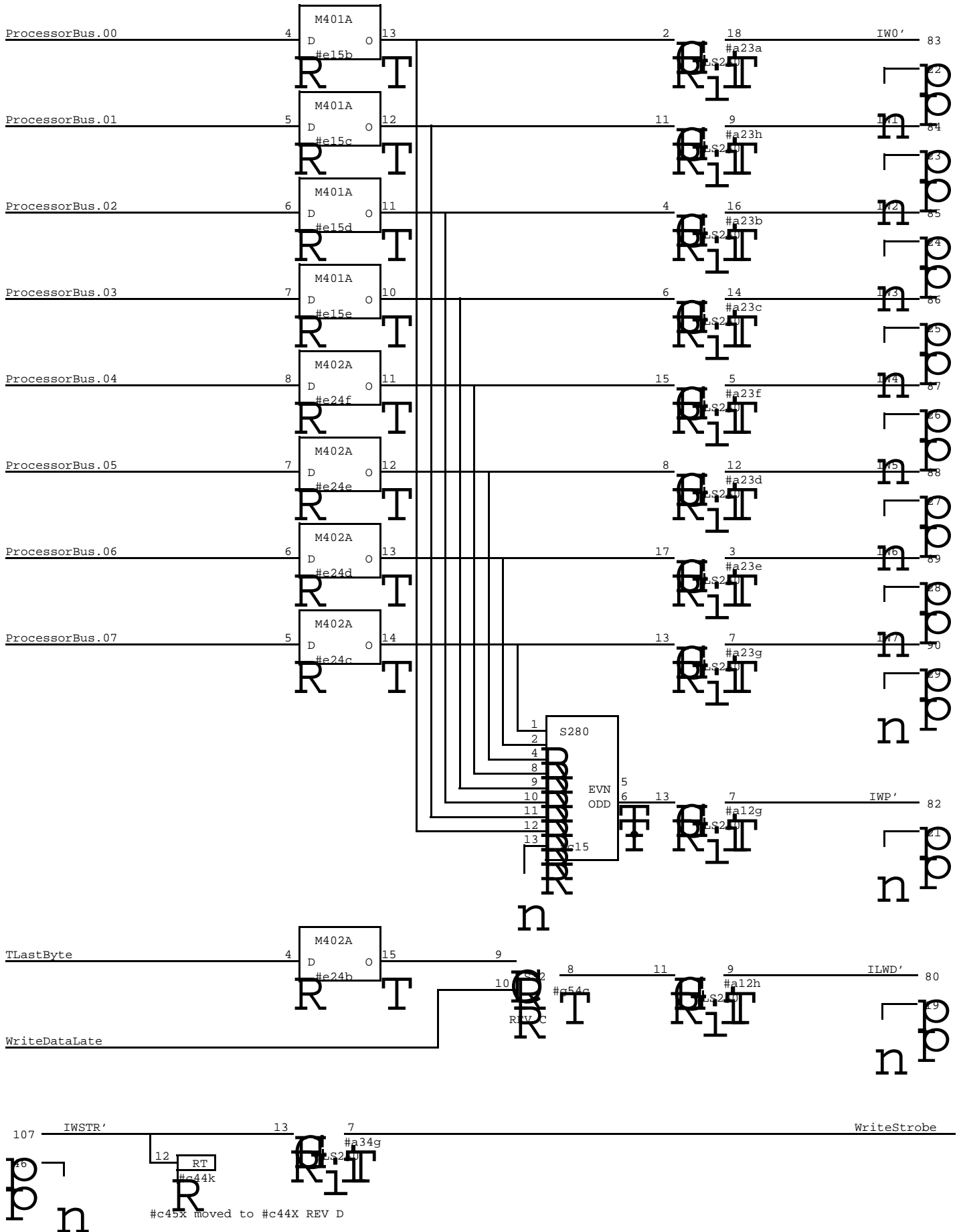


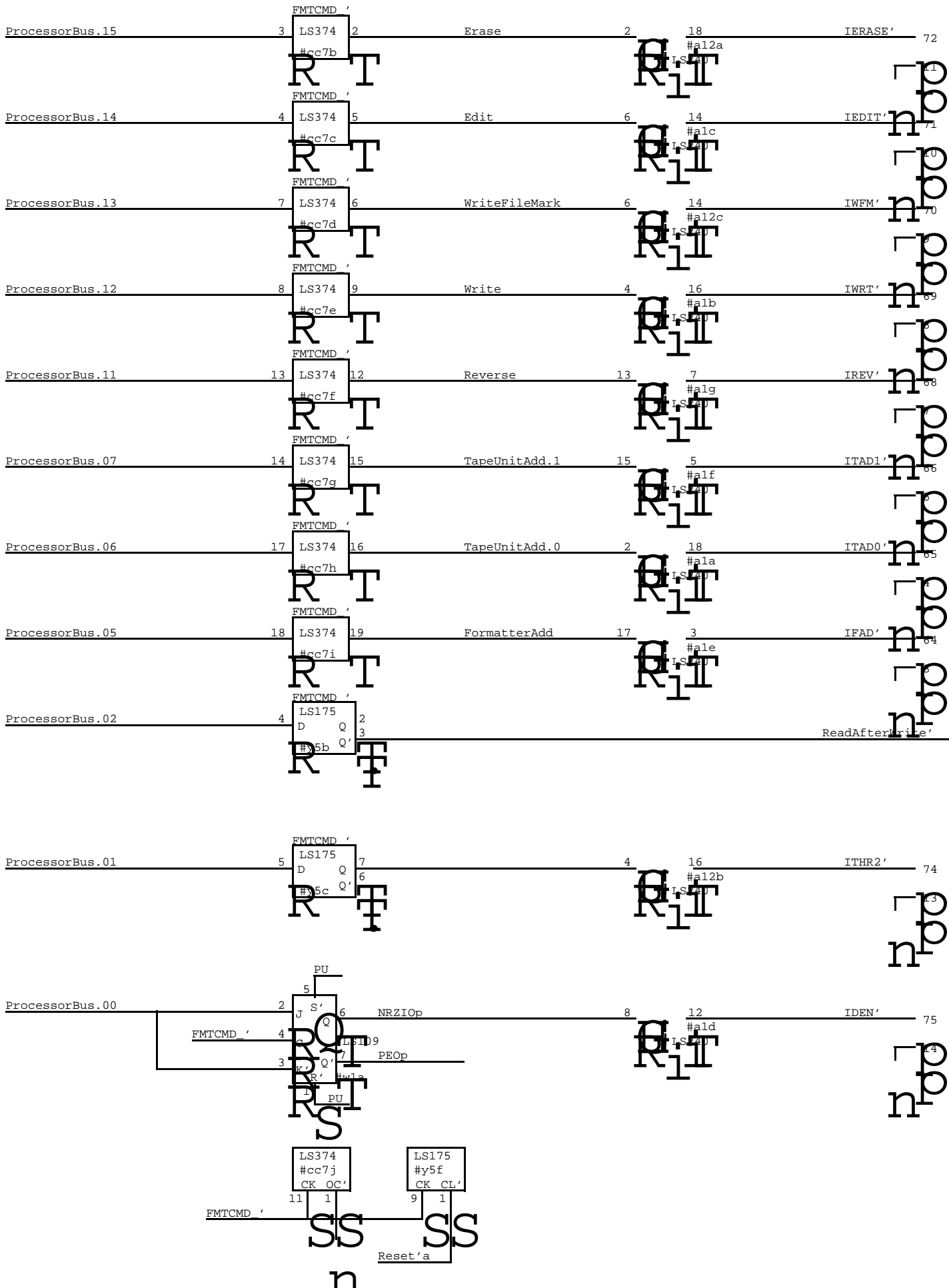
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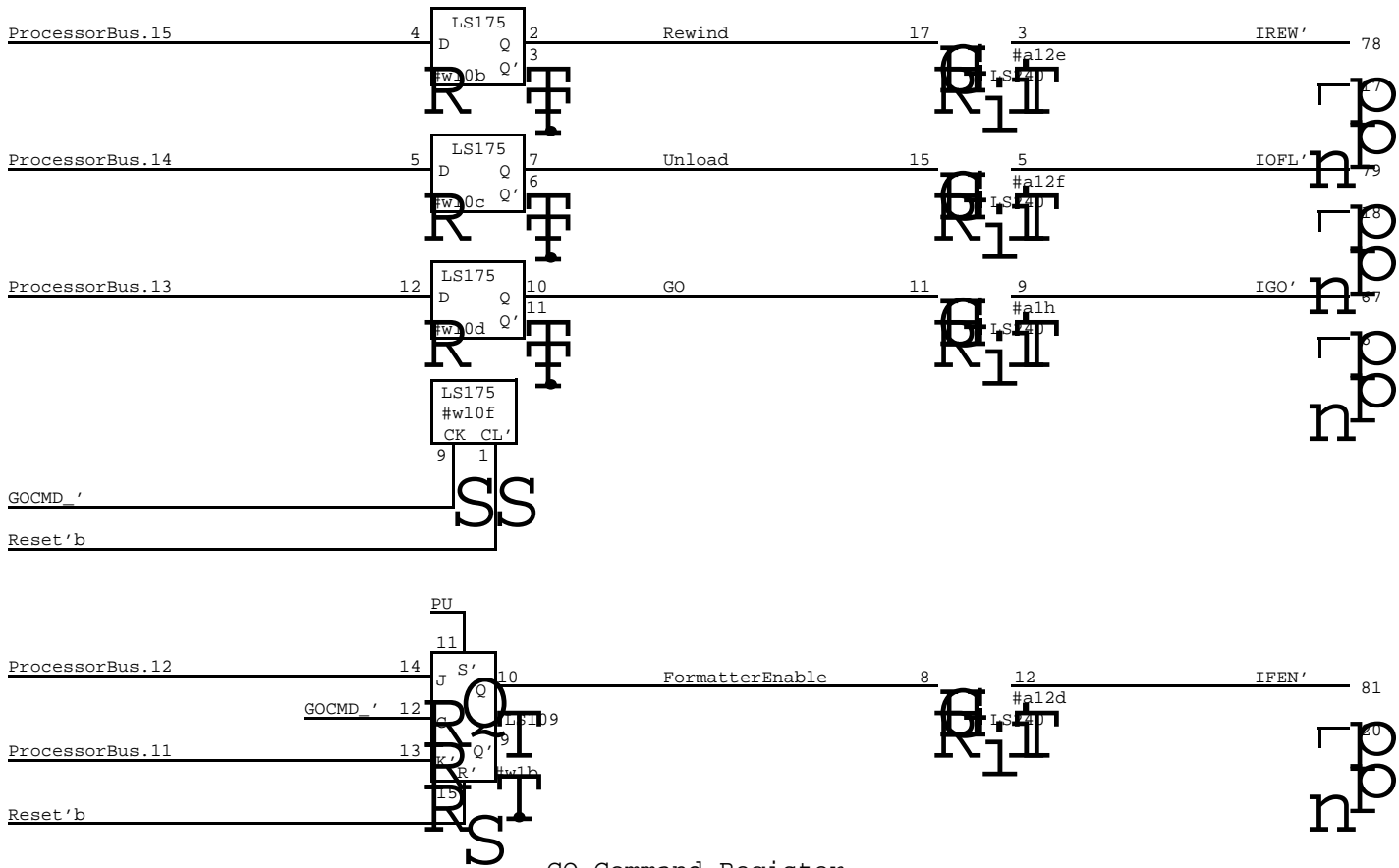


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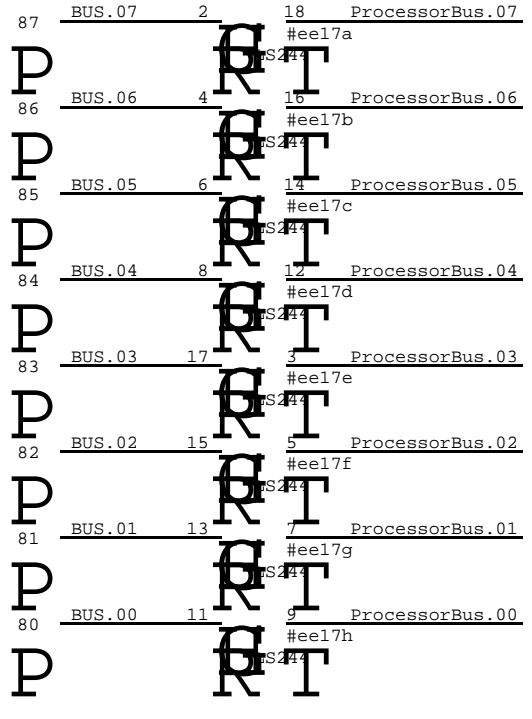
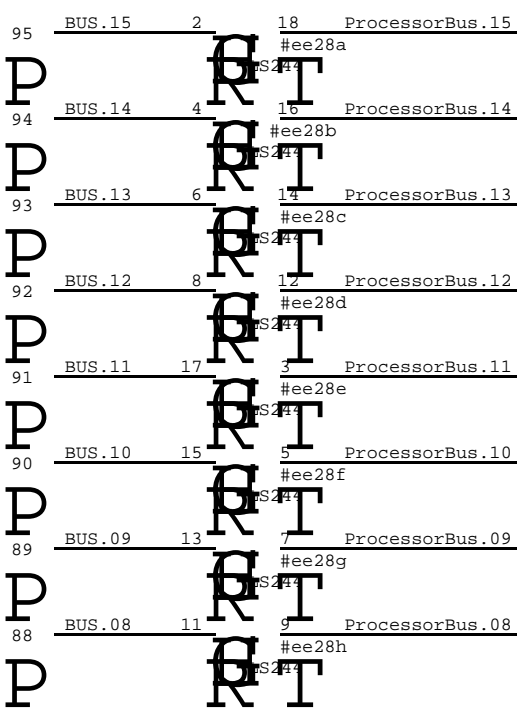






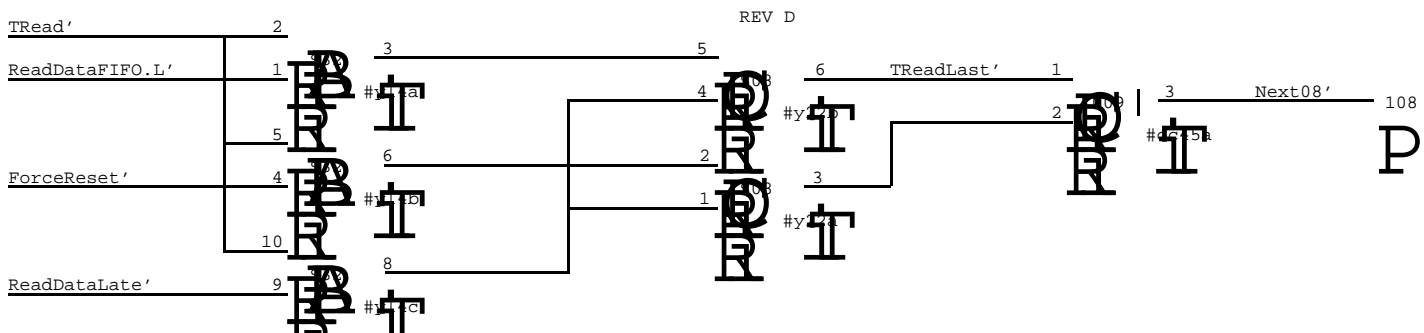
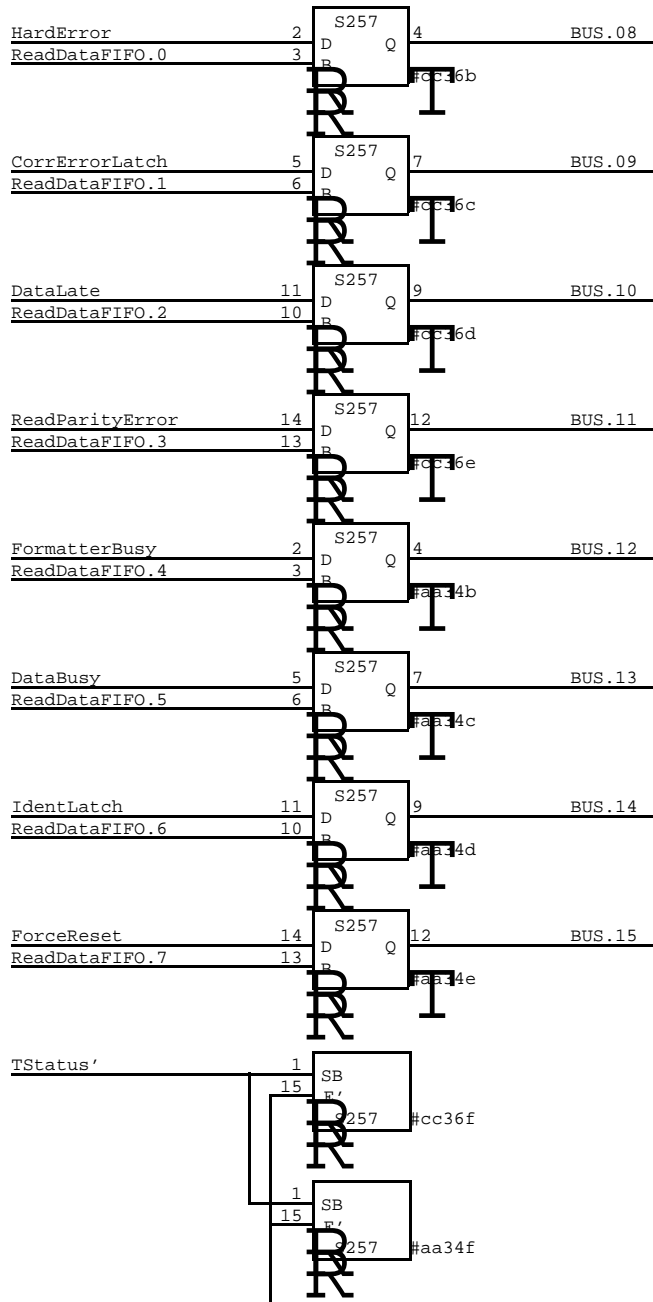
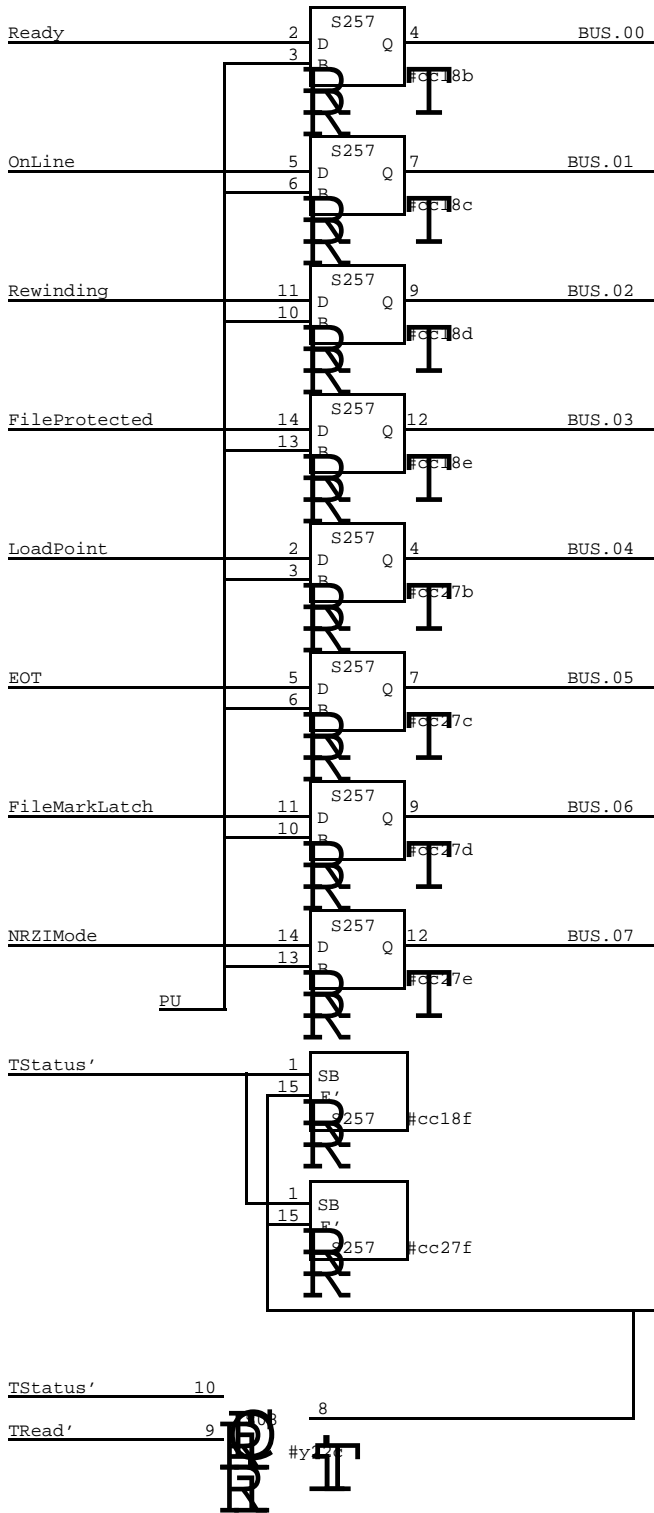


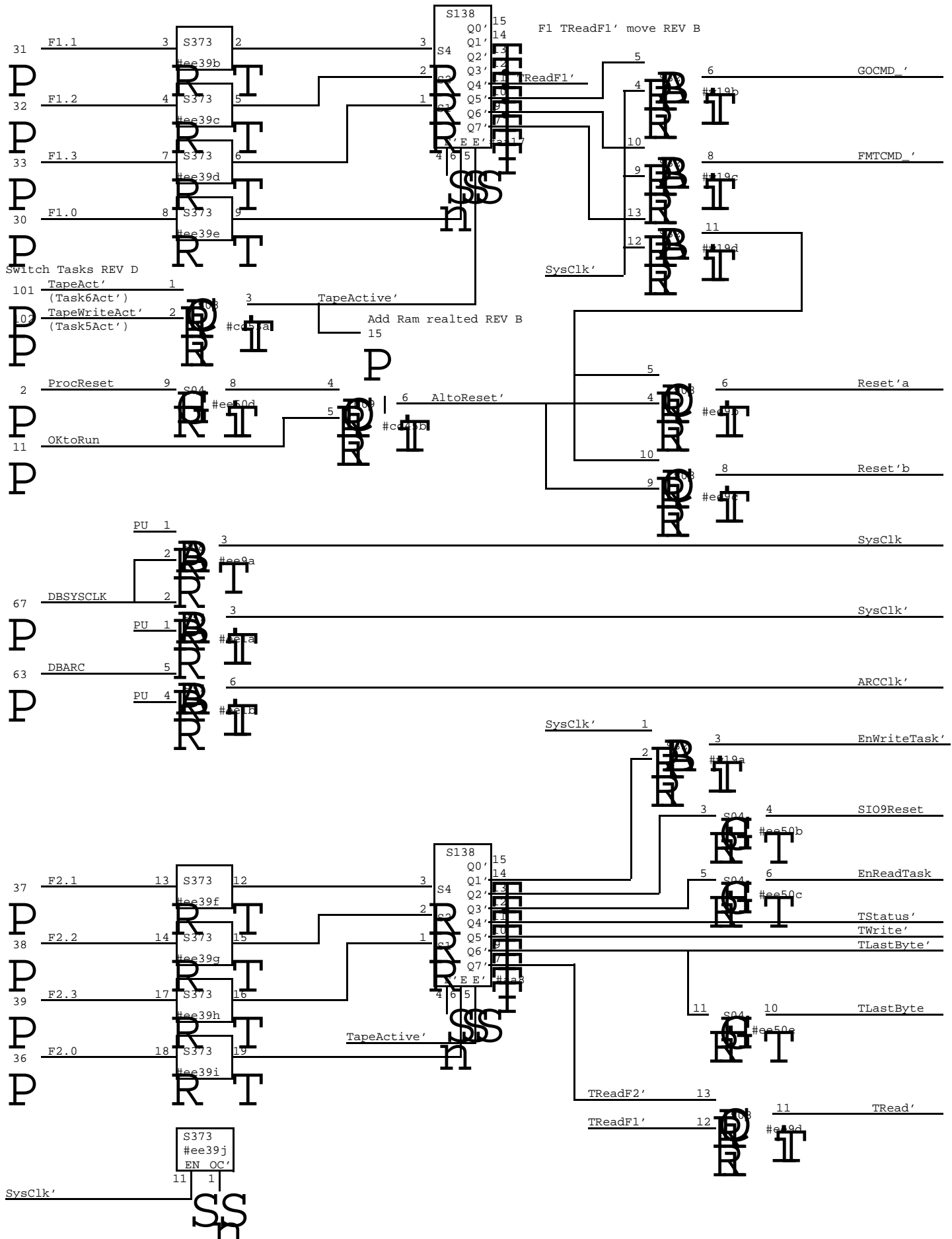
GO Command Register



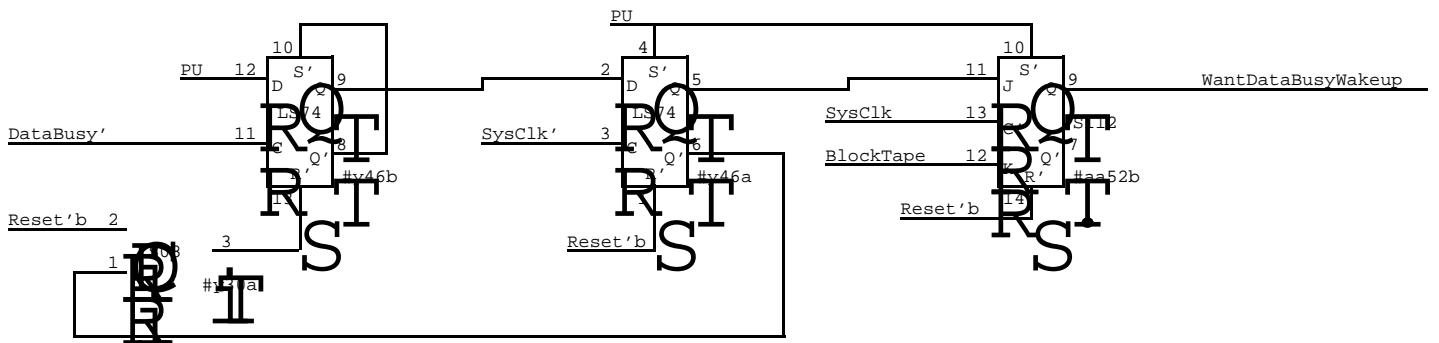
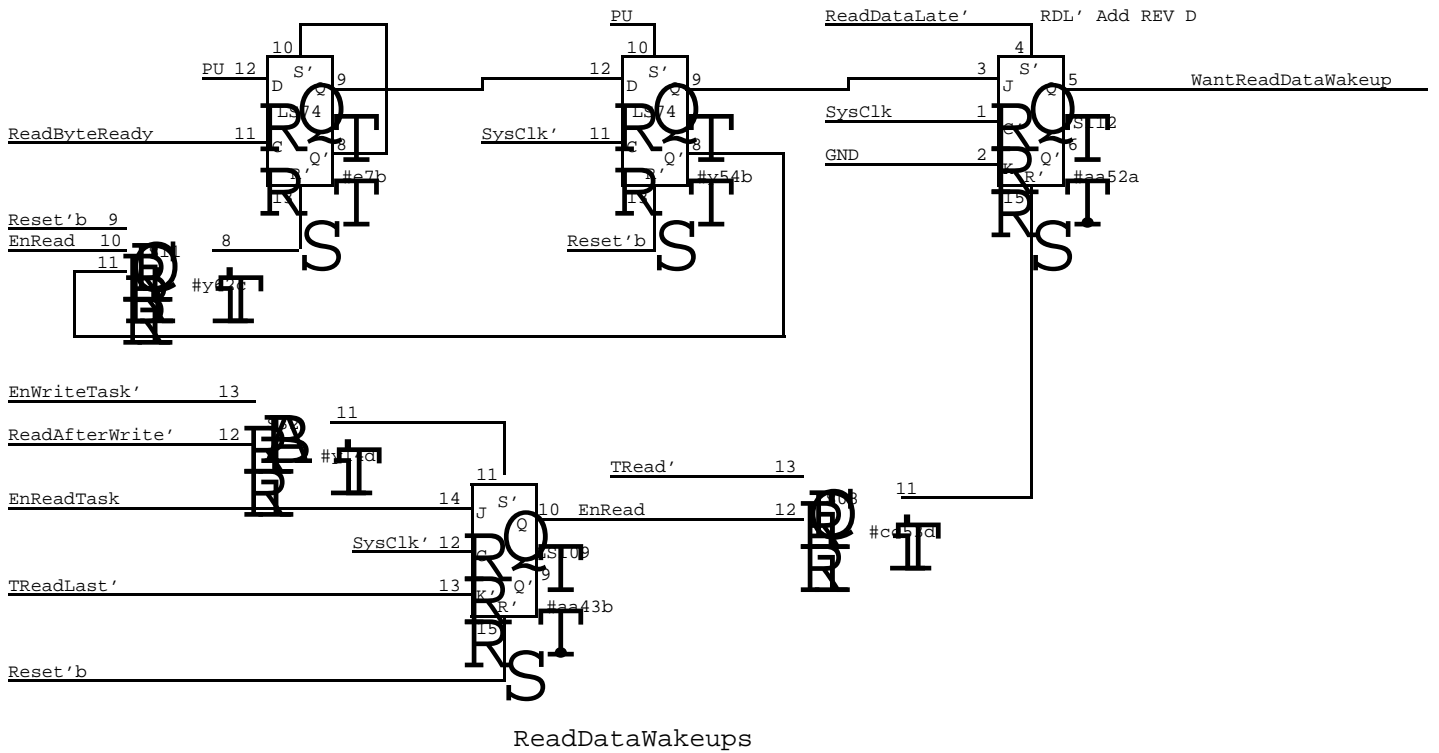
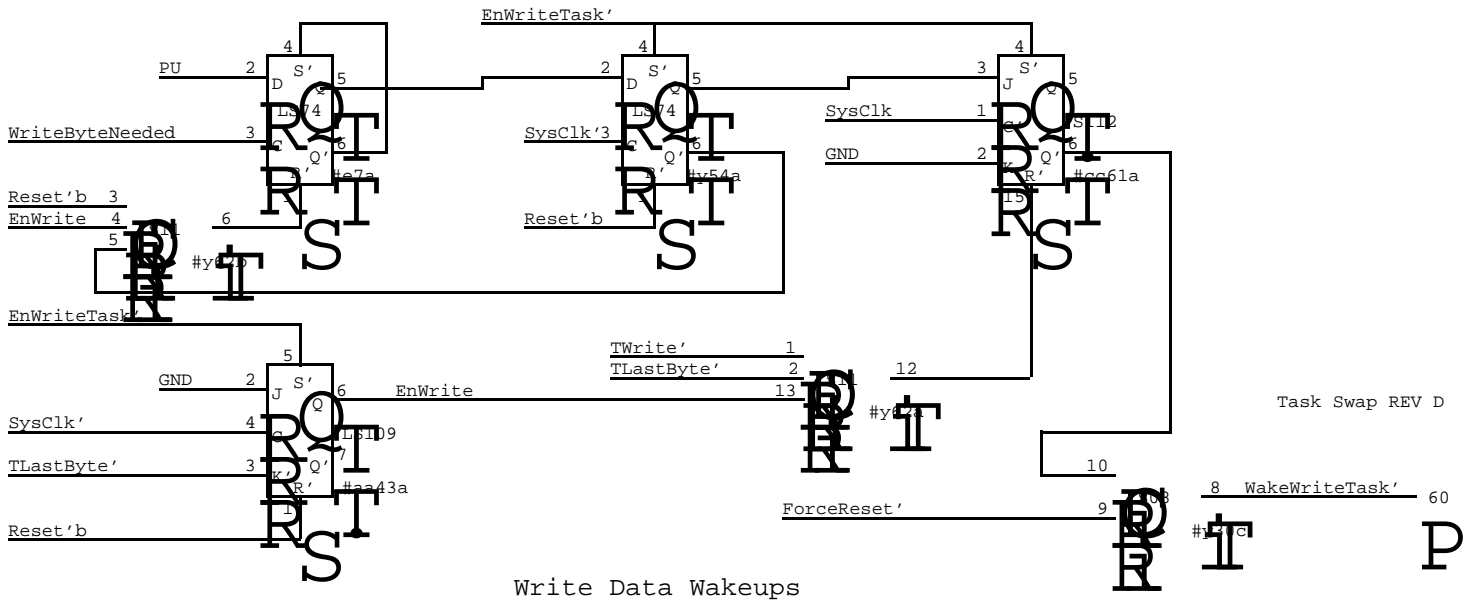
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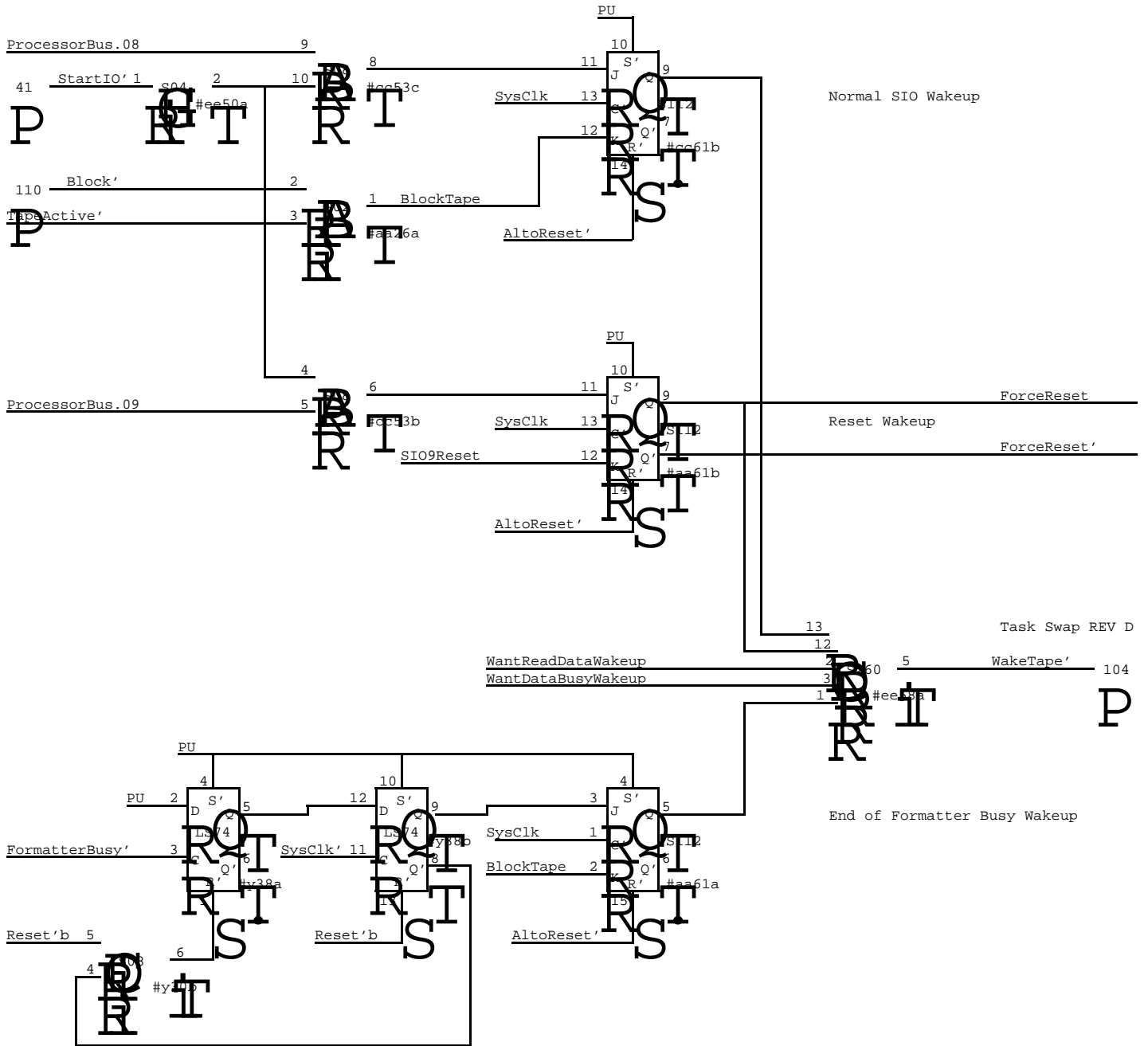
XEROX PARC/CSL	Project DDTape	GO Command Register Alto Bus Interface	File DDTape08.sil	Designer Tim Diebert	Rev D	Date 12/18/80	Page 09
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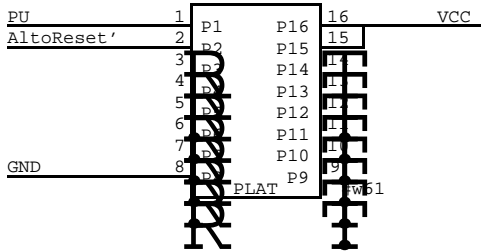
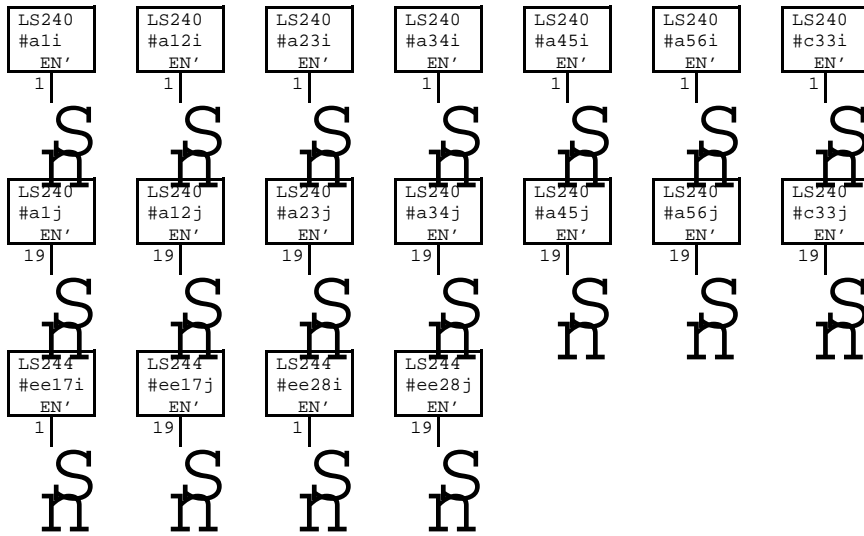




XEROX PARC/CSL	Project DDTape	Alto Processor Interface	File DDTape10.sil	Designer Tim Diebert	Rev D	Date 2/12/81	Page 11
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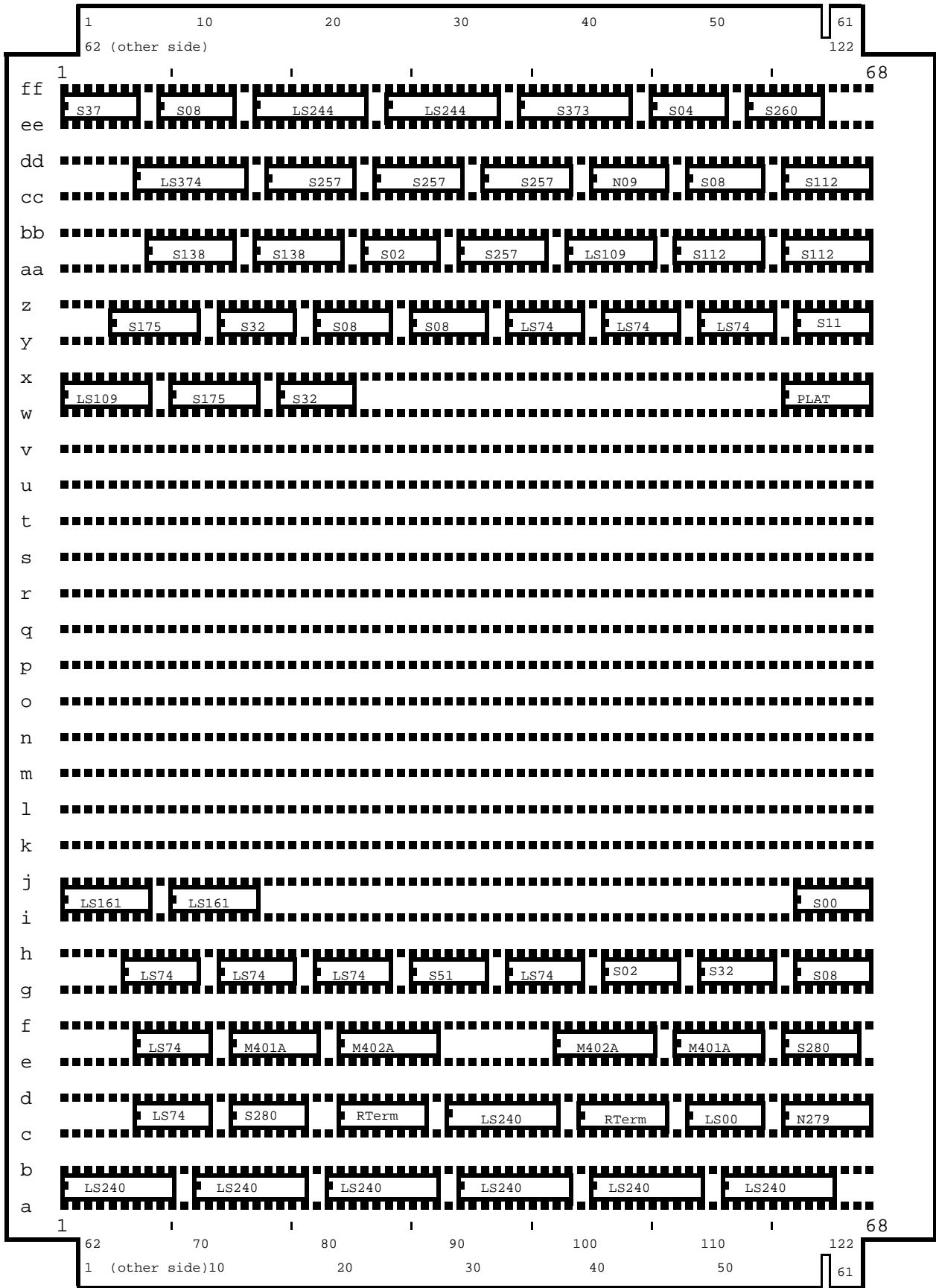






1k ohm resistor from 1 to 16
 330 ohm resistor from 2 to 15

E D G E C O N N E C T O R



C A B L E C O N N E C T O R

Misc Clean up REV D

As viewed from the component side

Load .01uf caps all available locations near chips
Install heavy ground connections from edge to power p.

XEROX PARC/CSL	Project DDTape	Reference Layout	File DDTape14.sil	Designer Tim Diebert	Rev D	Date 2/12/81	Page 15
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