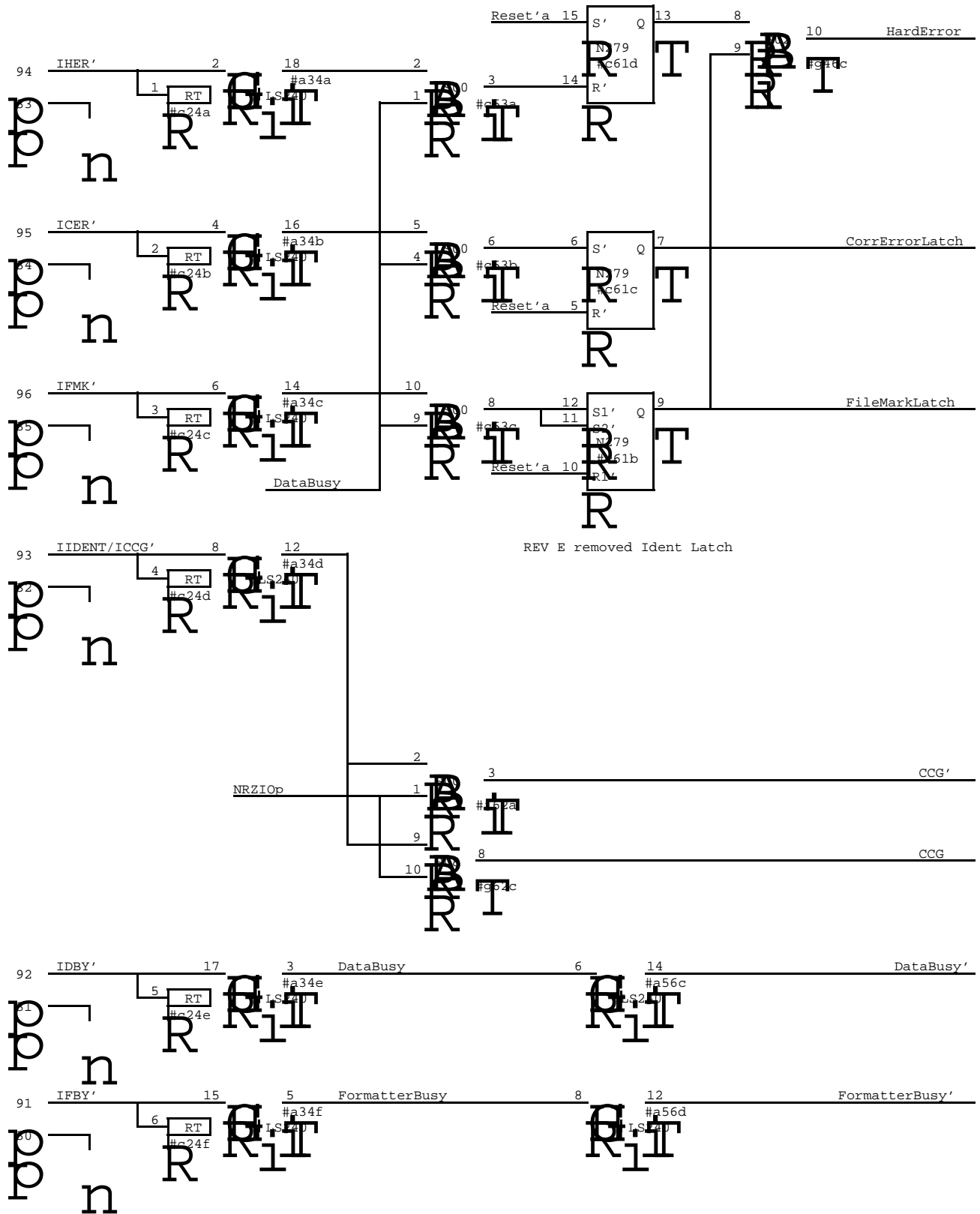
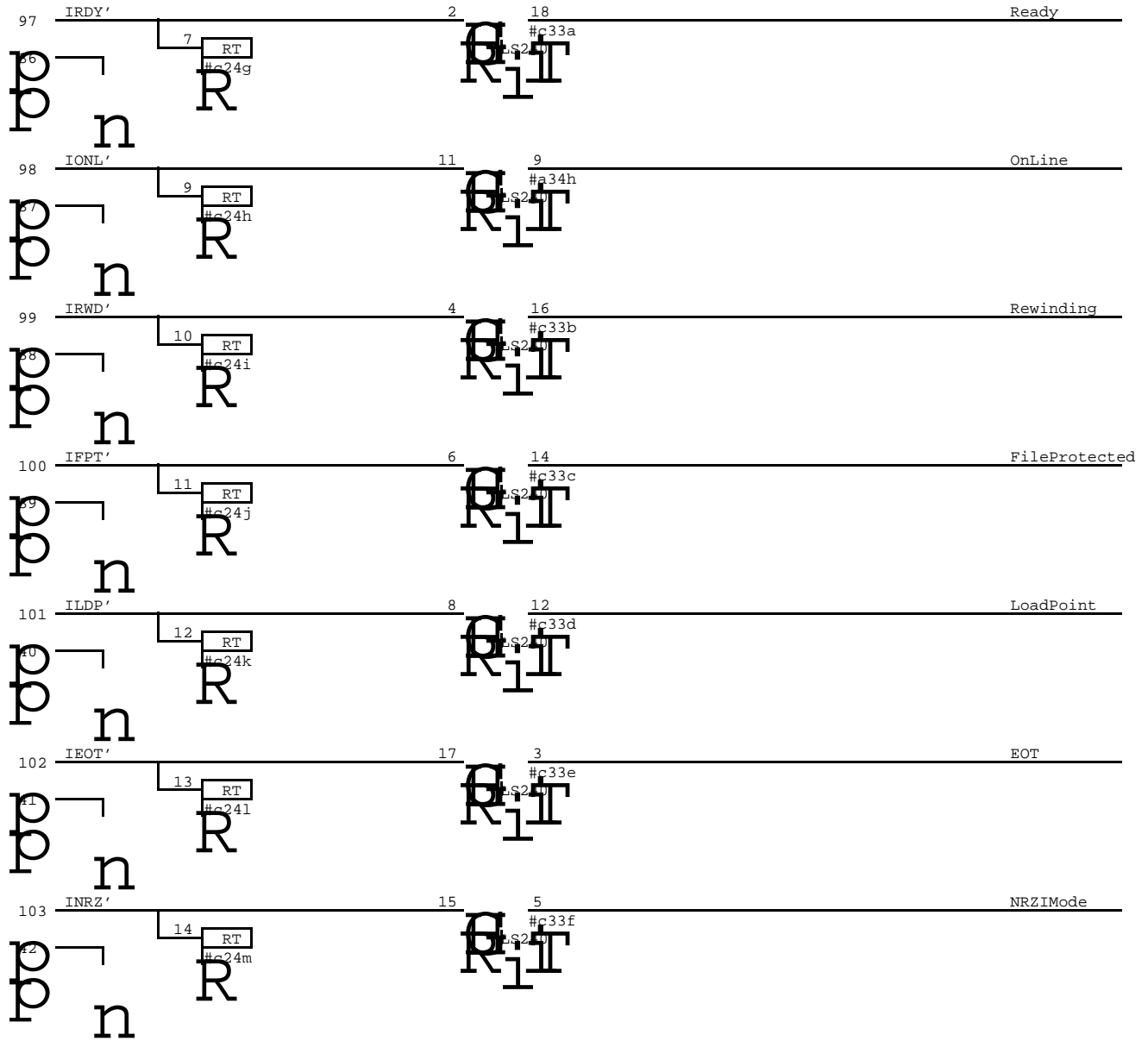


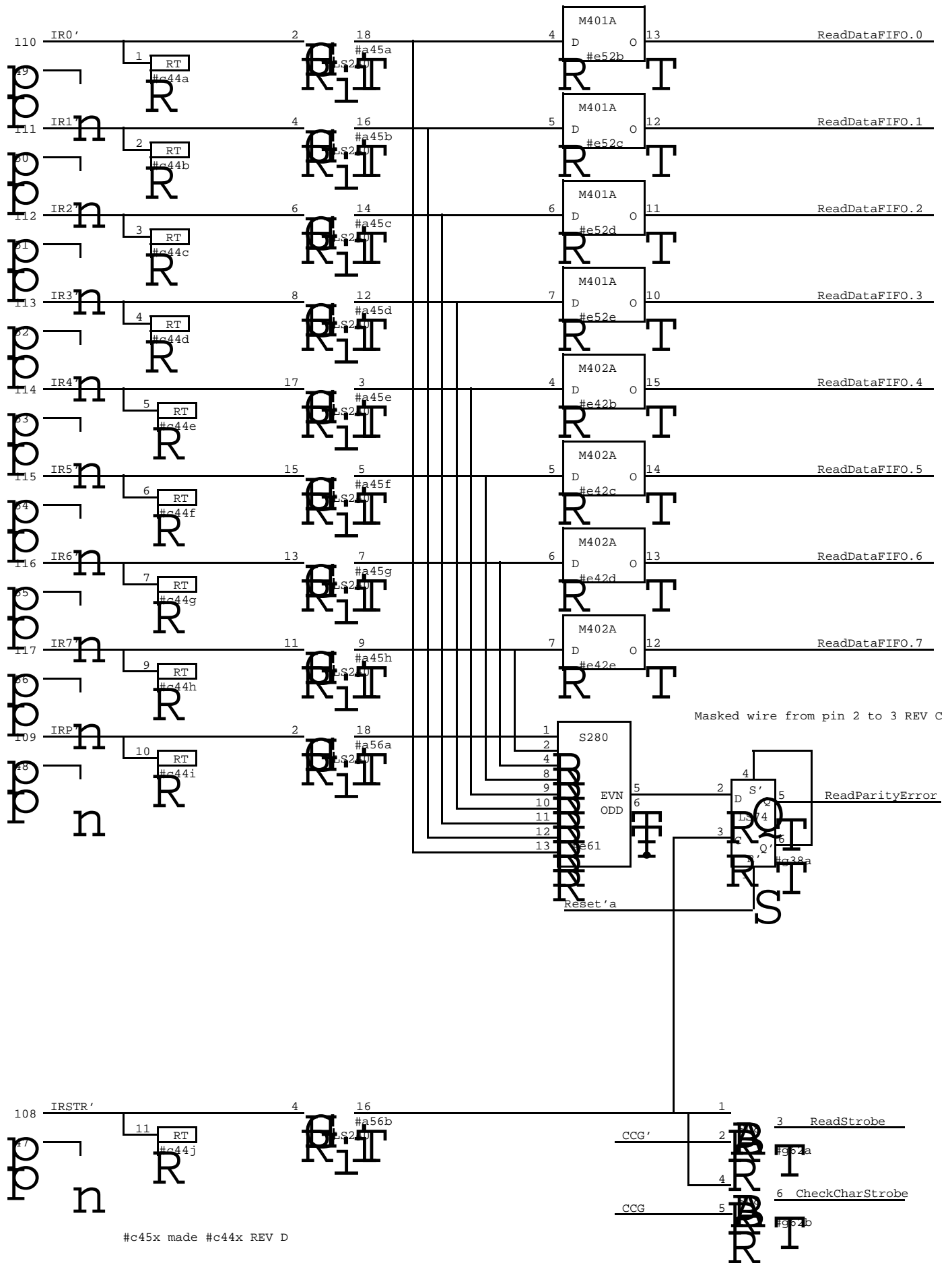
A L T O   D U A L   D E N S I T Y  
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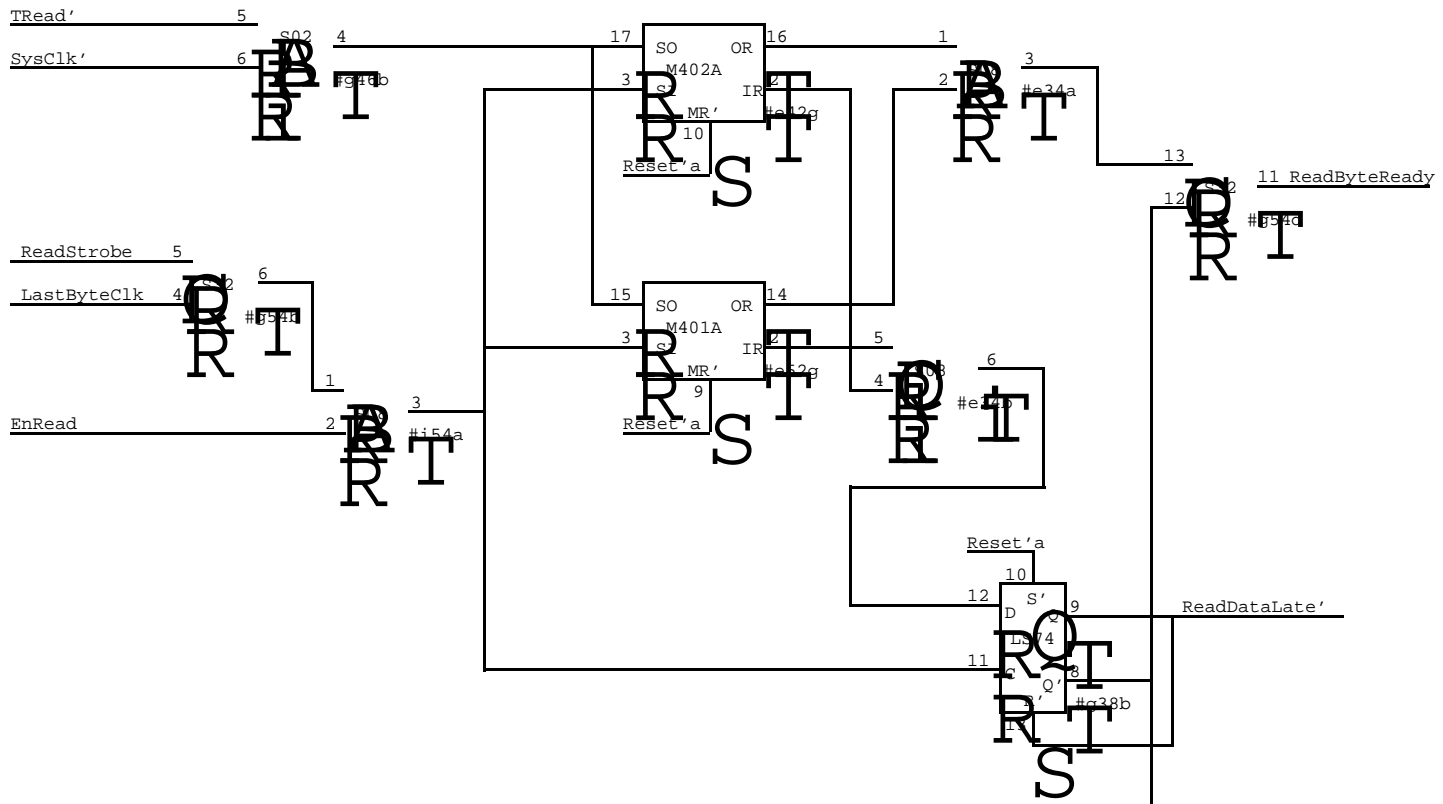
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| Formatter Status _____             | 0 1         |
| Tape Unit Status _____             | 0 2         |
| Read Data Interface and FIEO _____ | 0 3         |
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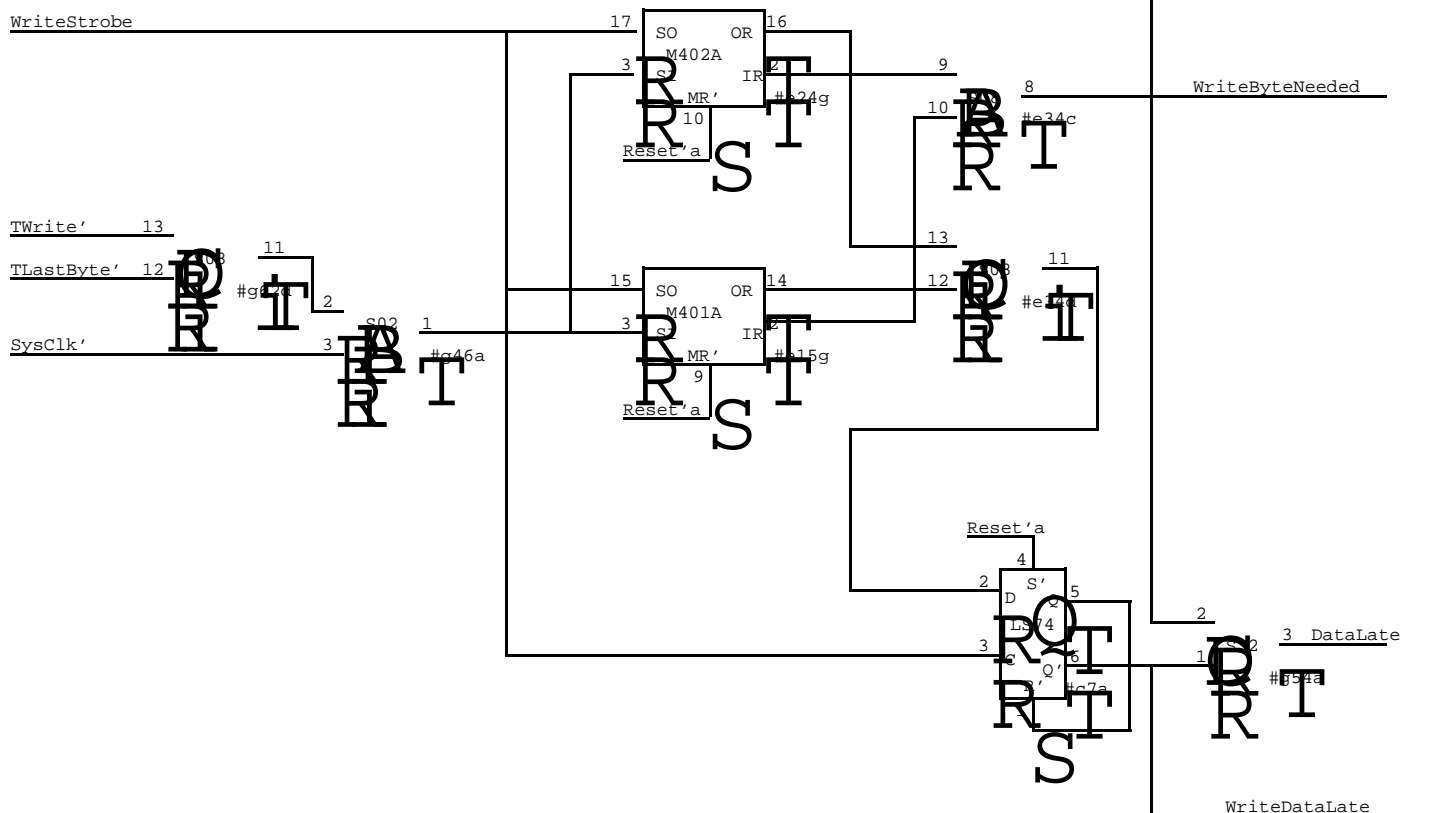


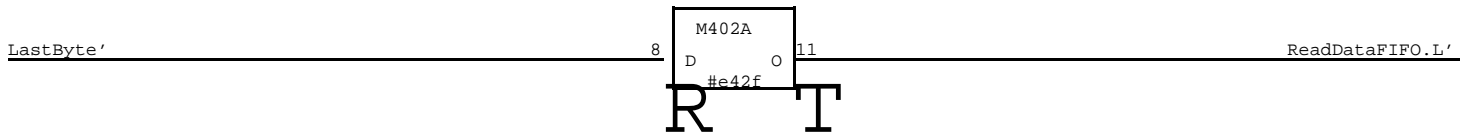
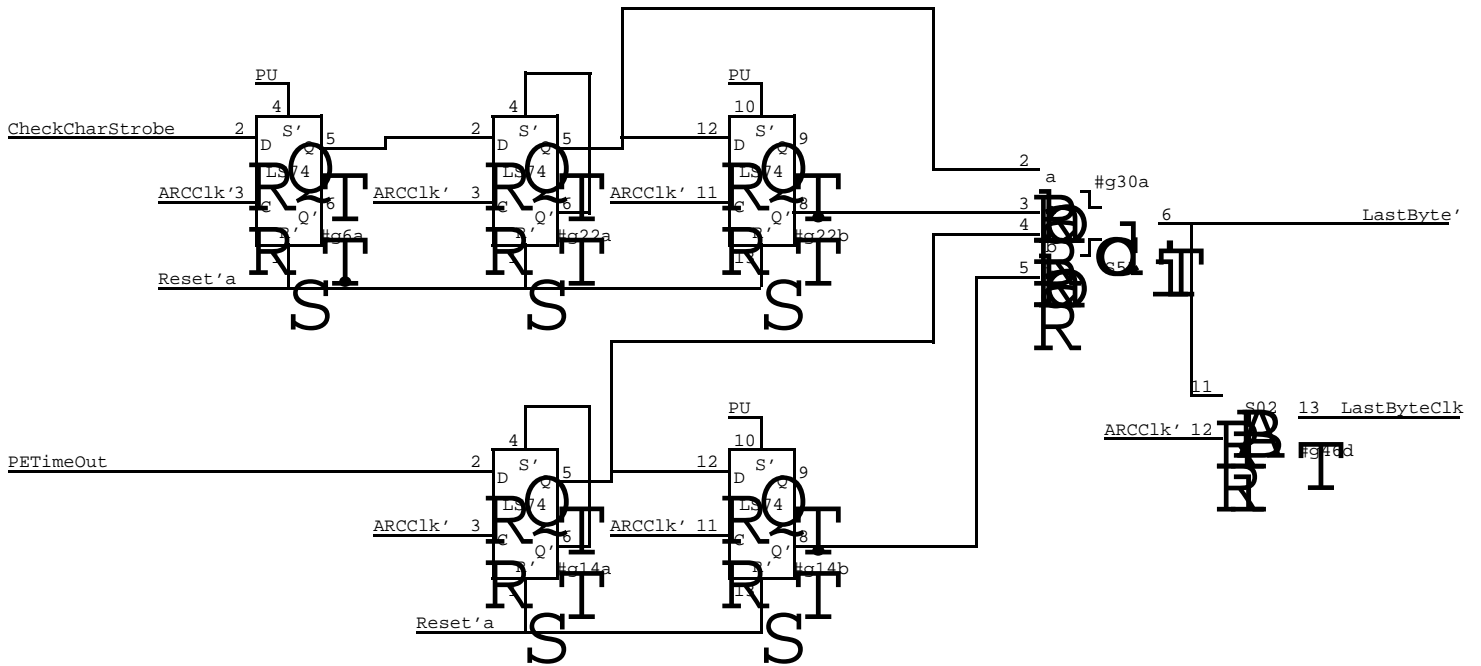
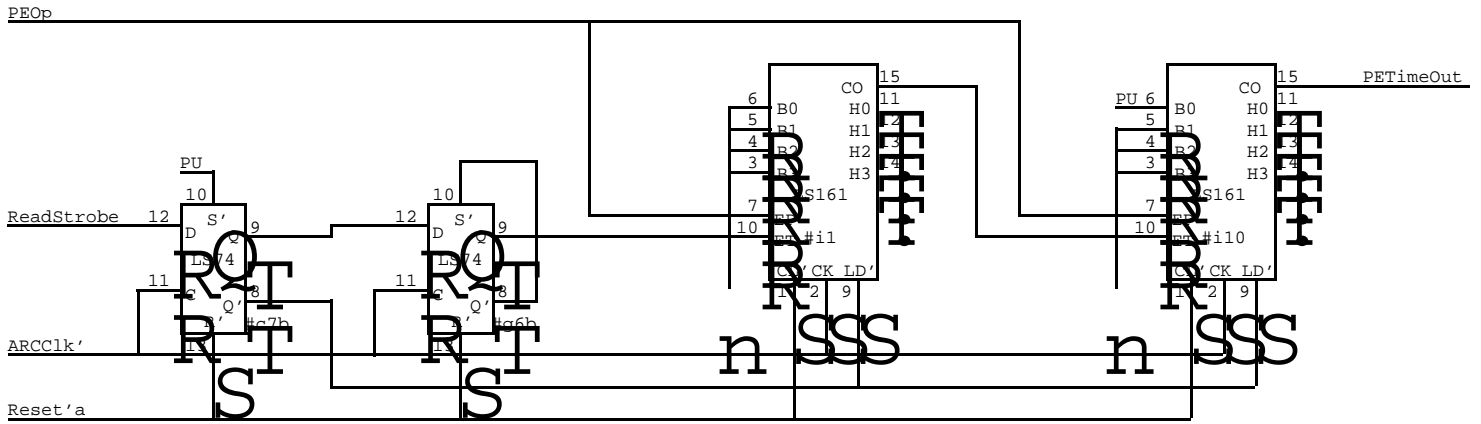


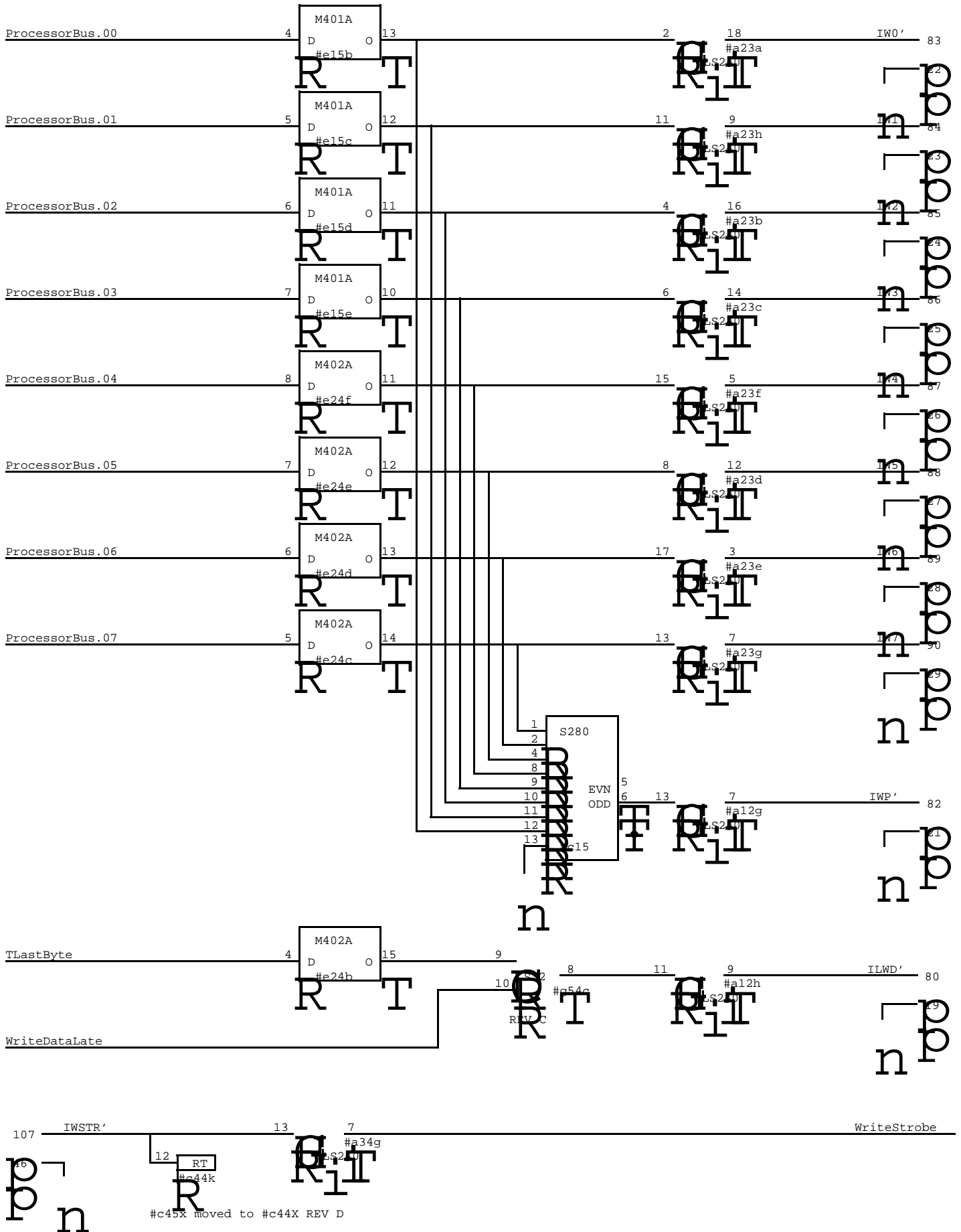
#c45x made #c44x REV D

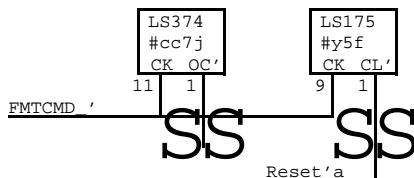
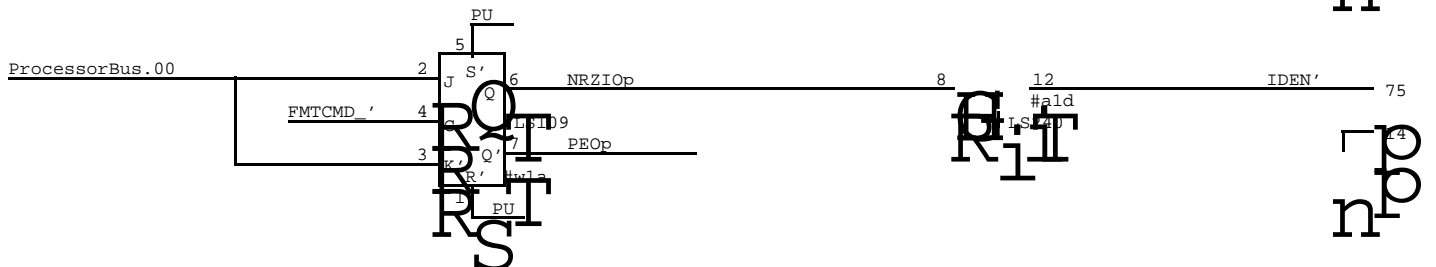
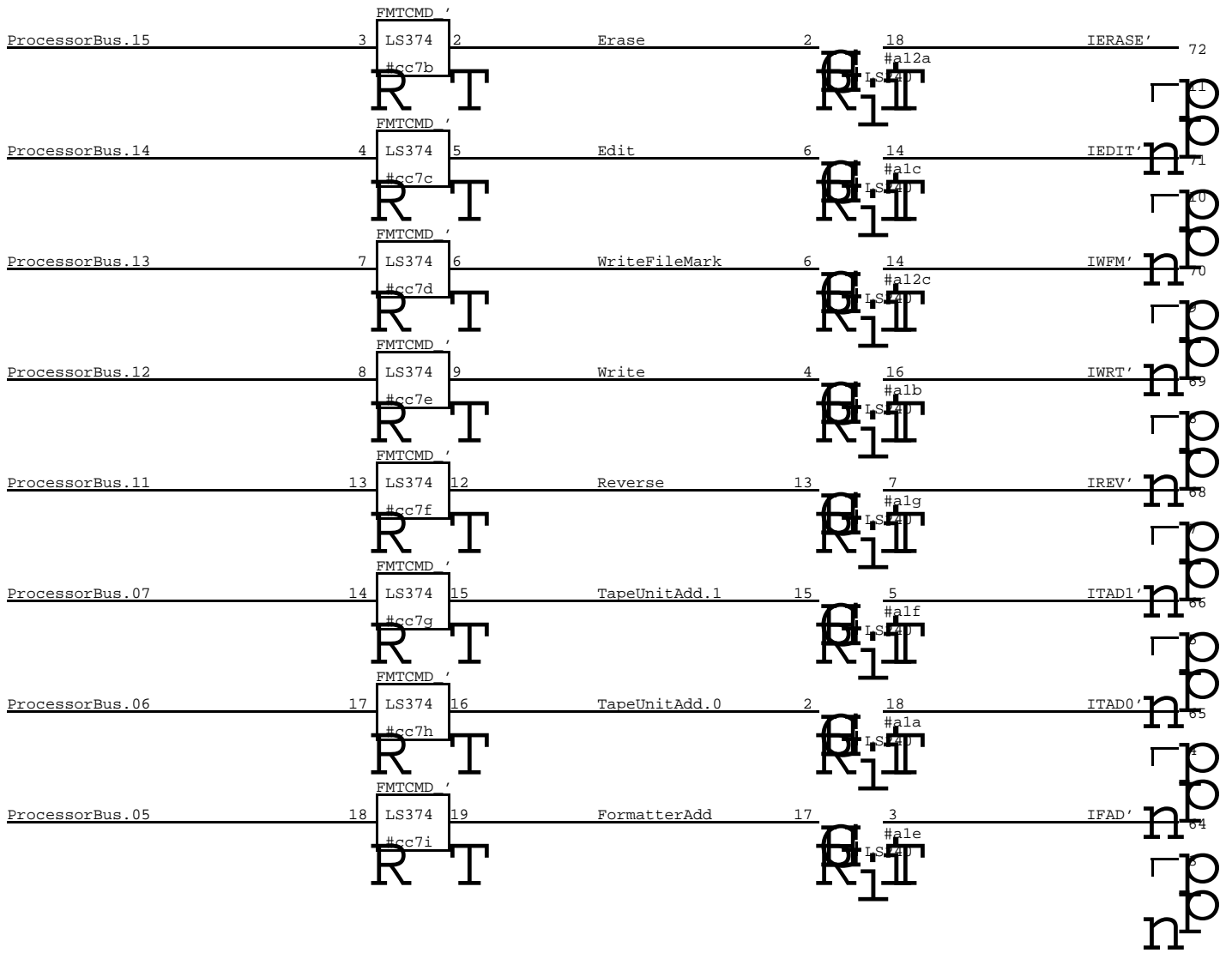


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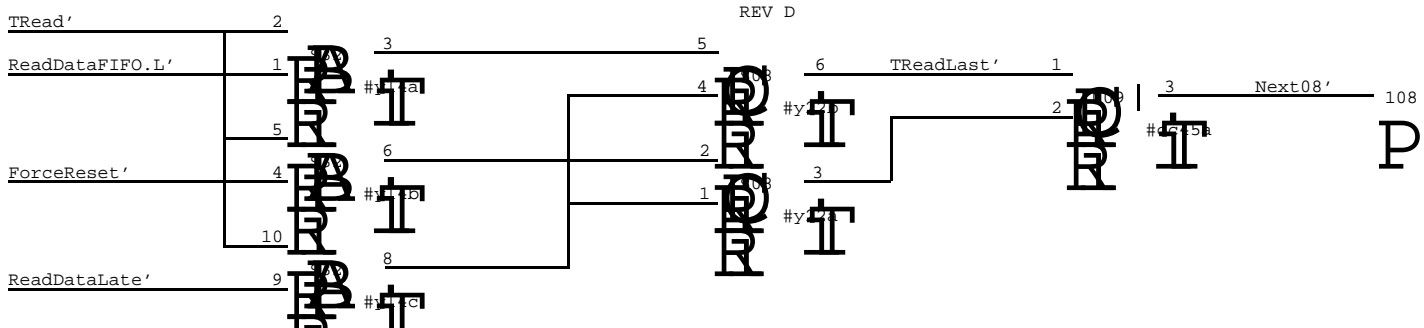
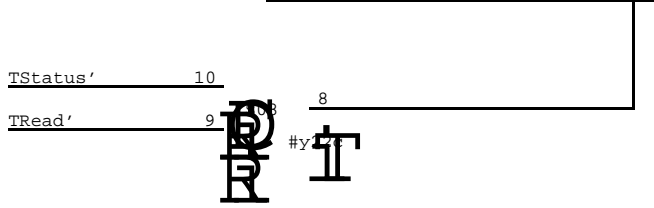
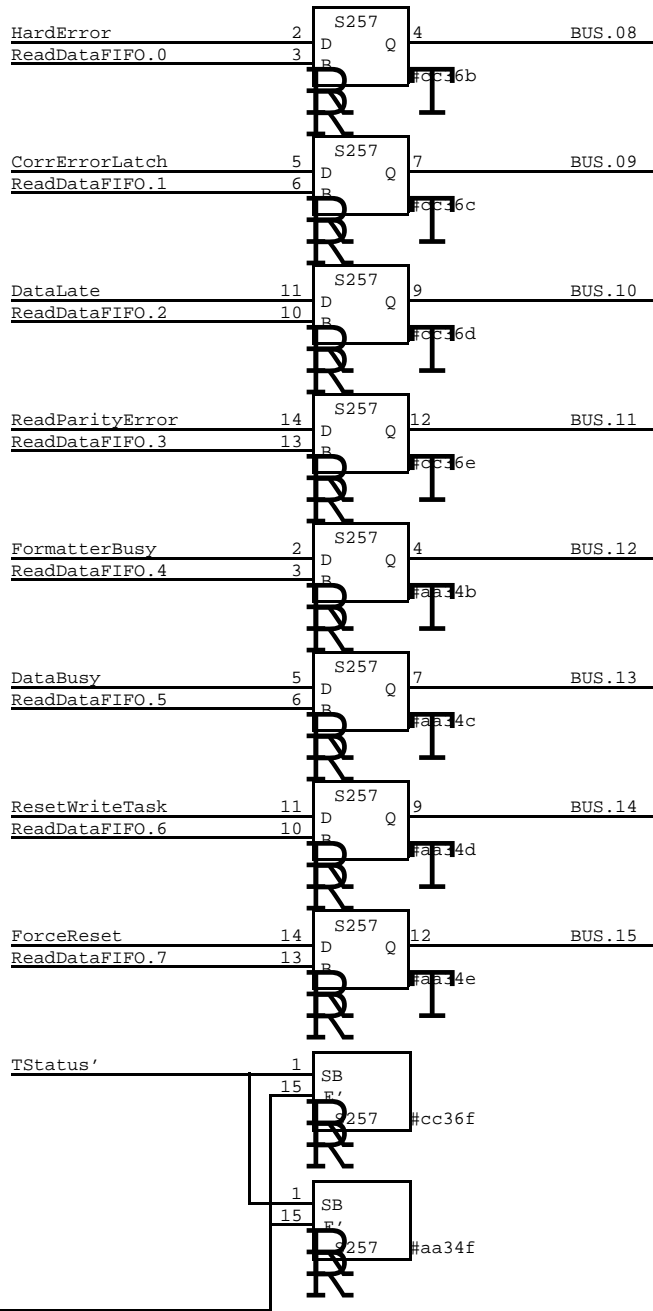
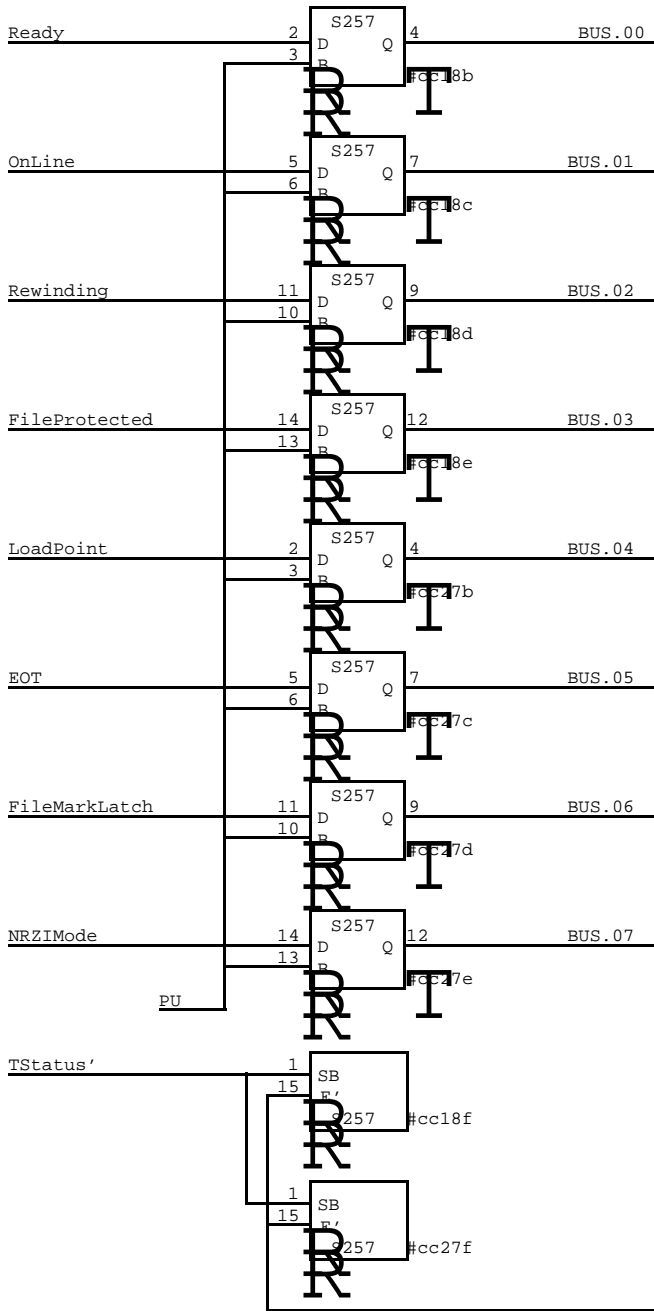


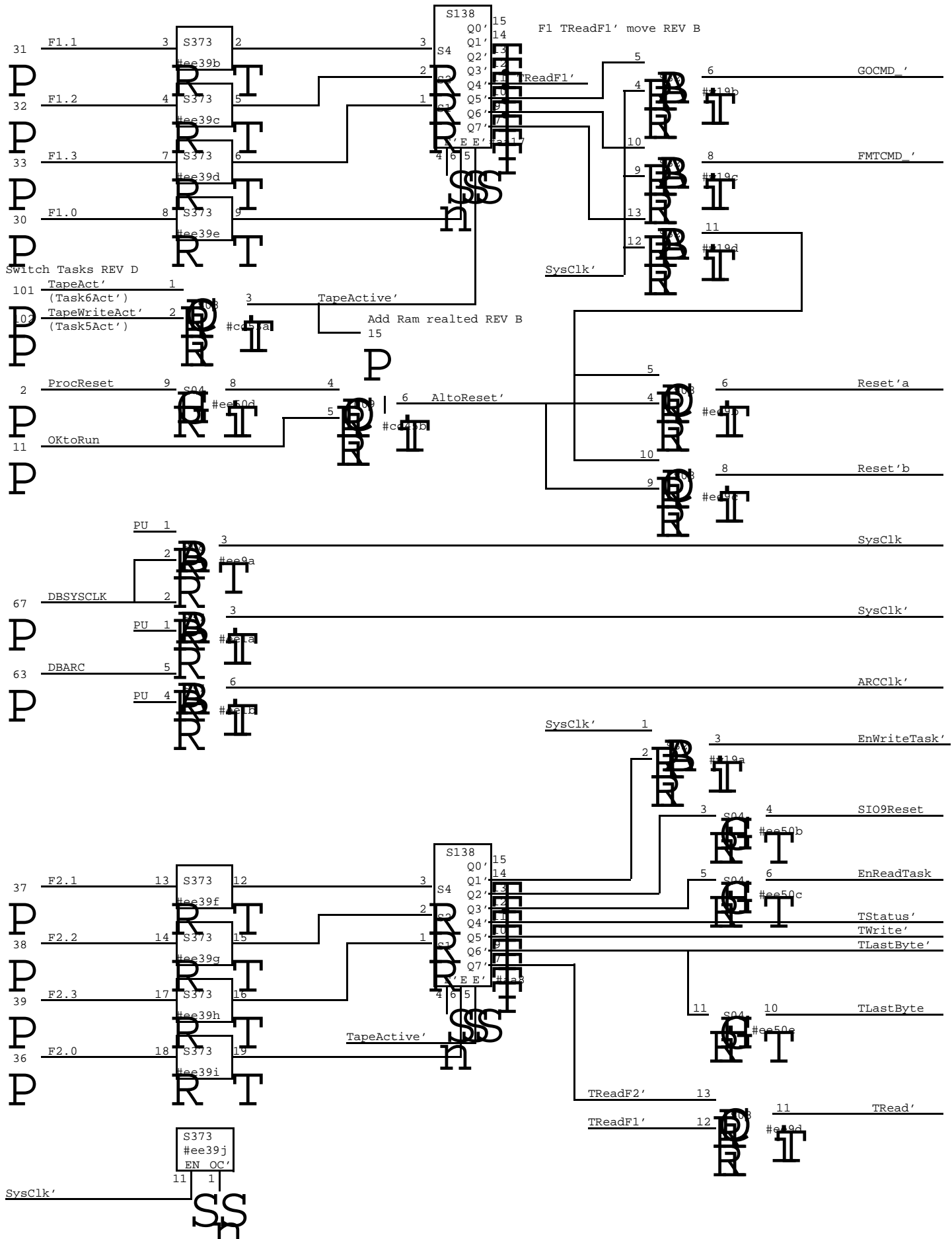


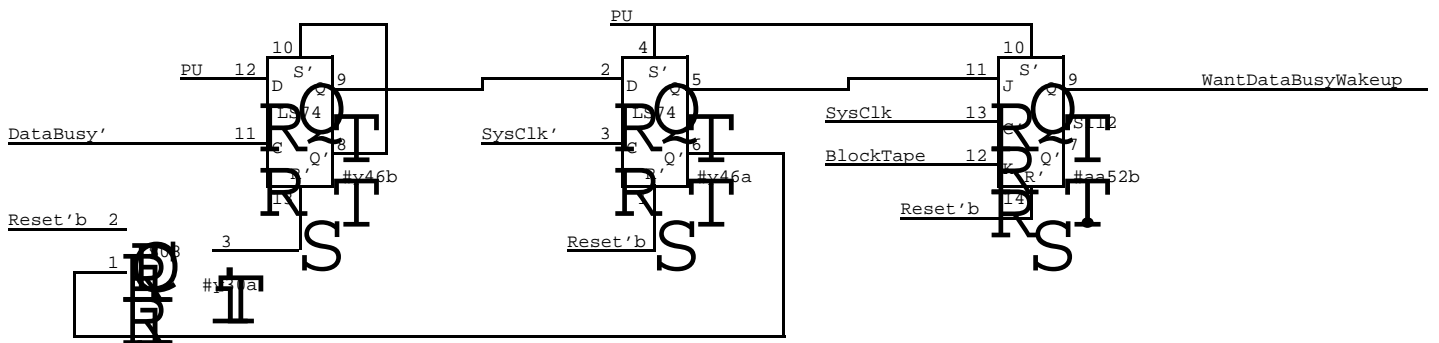
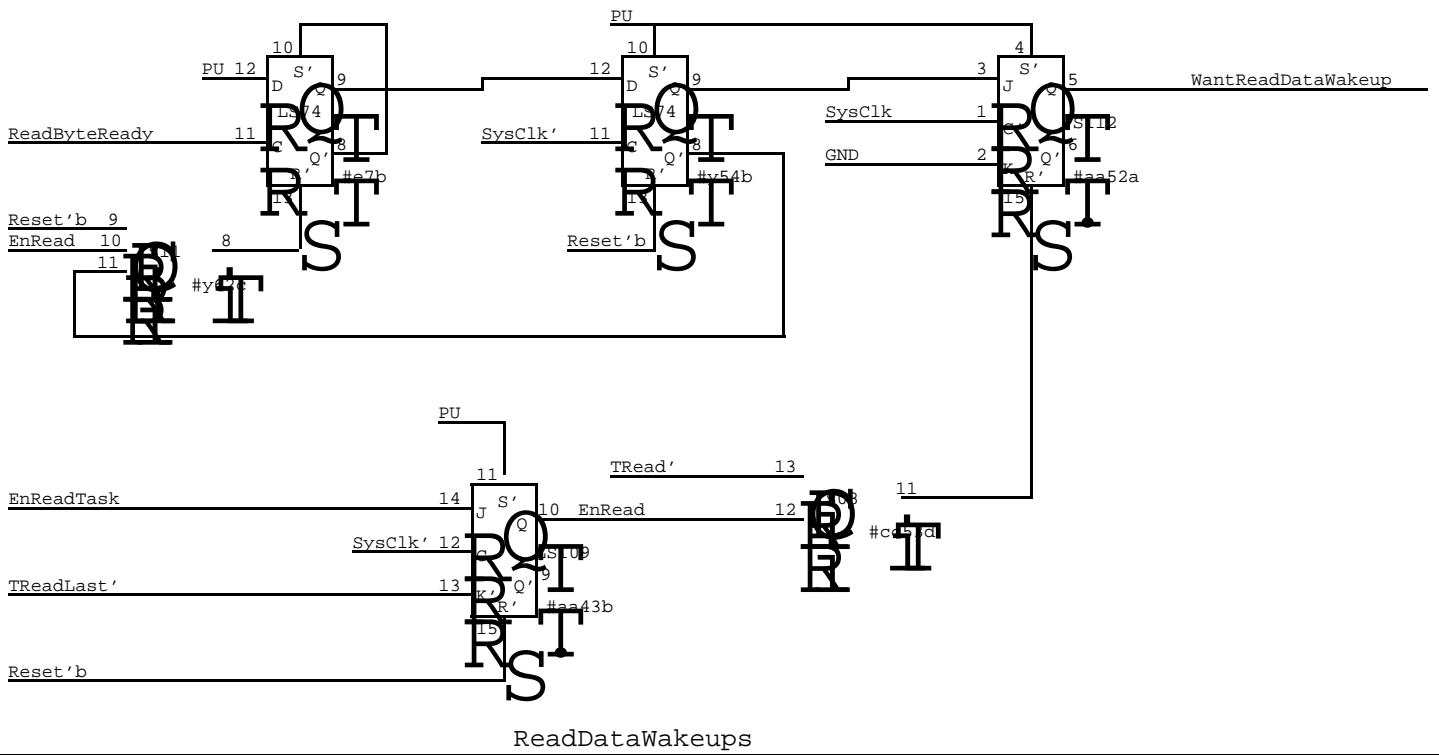
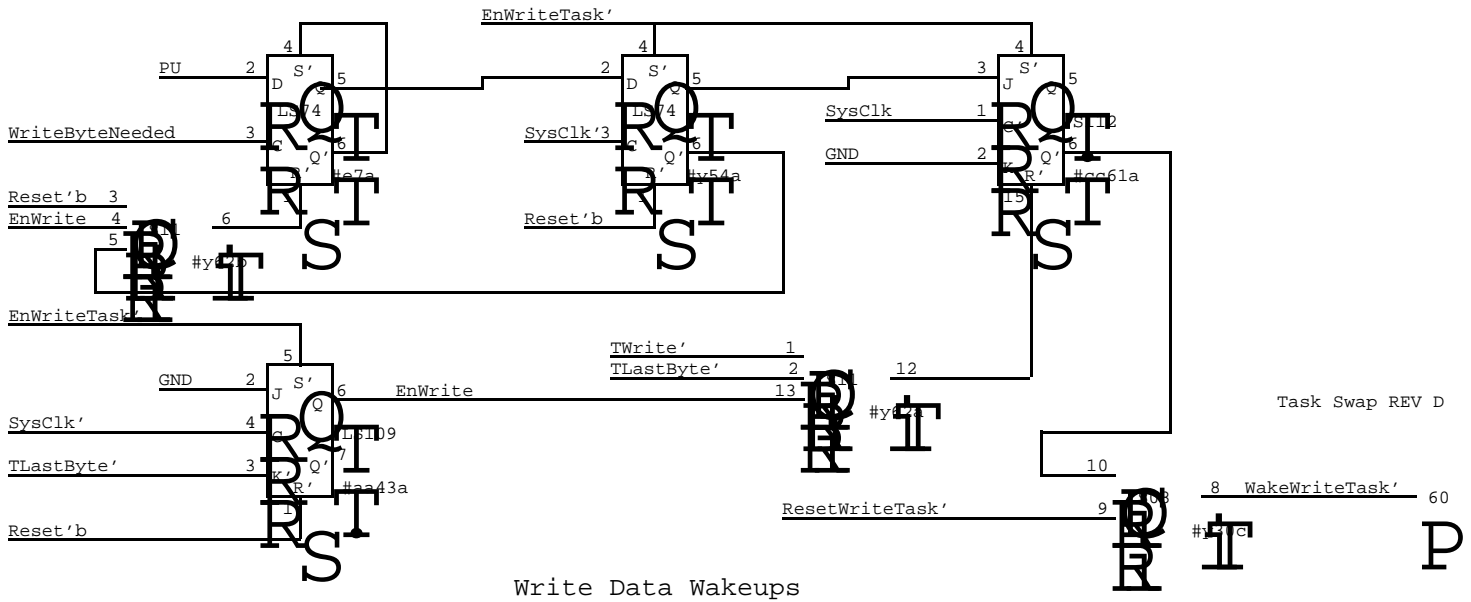




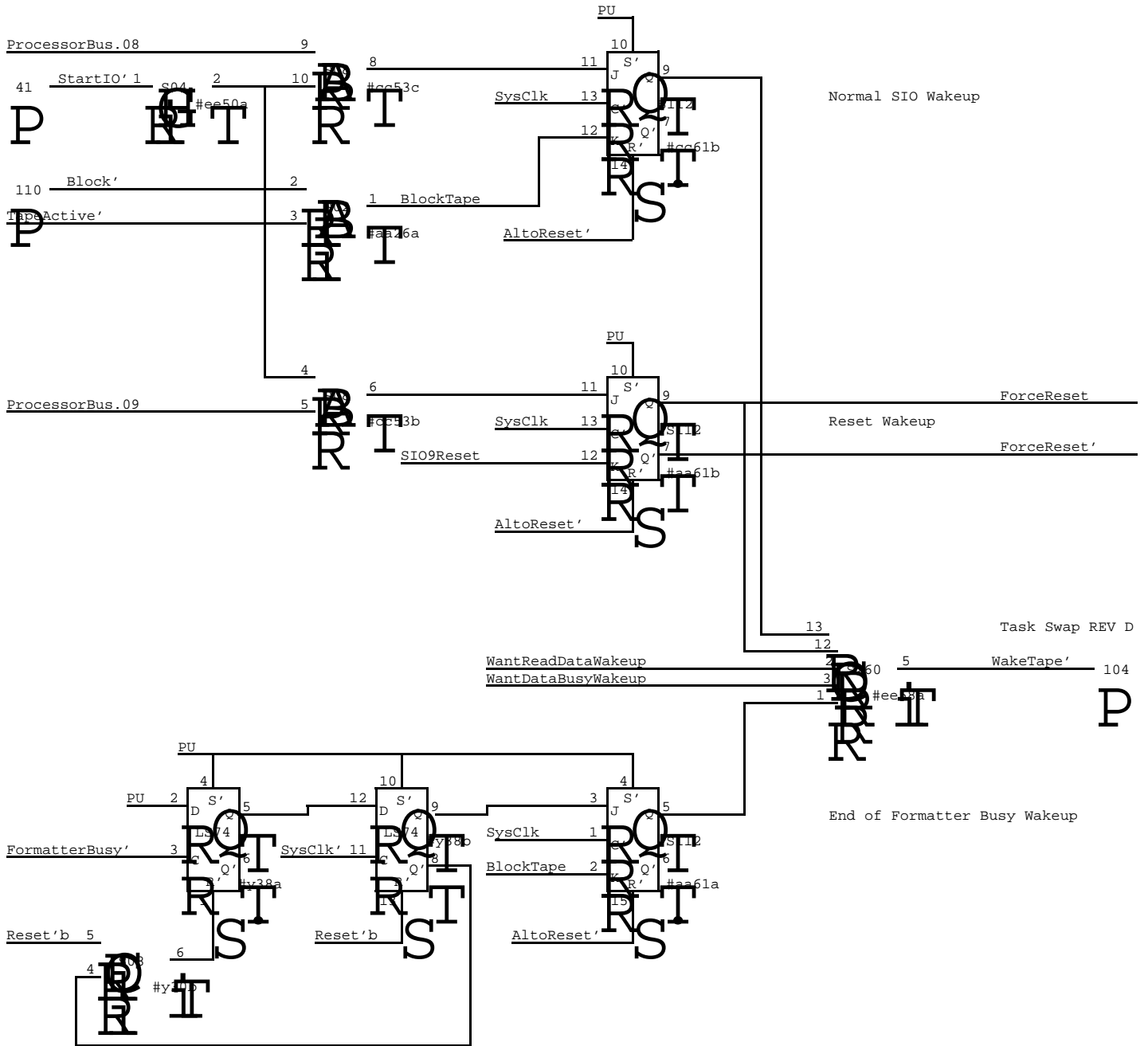


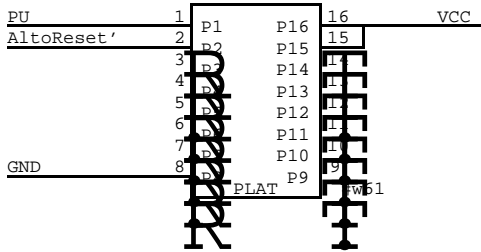
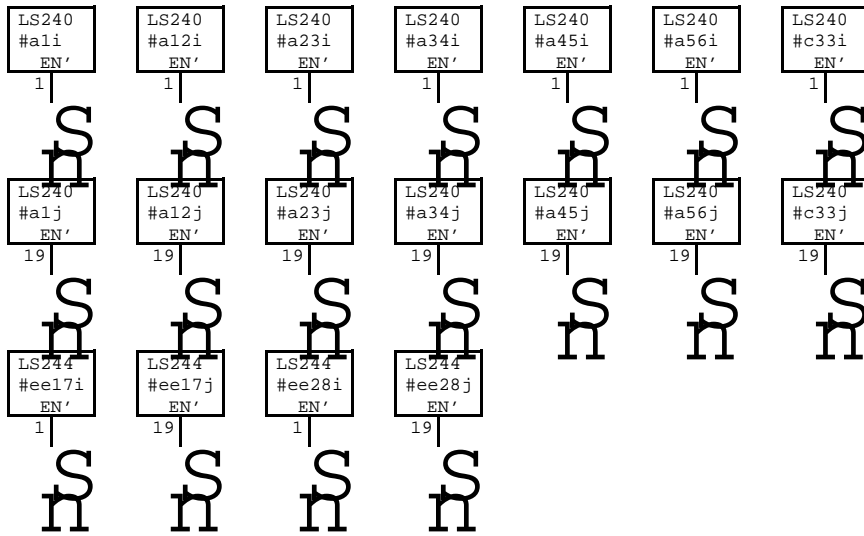






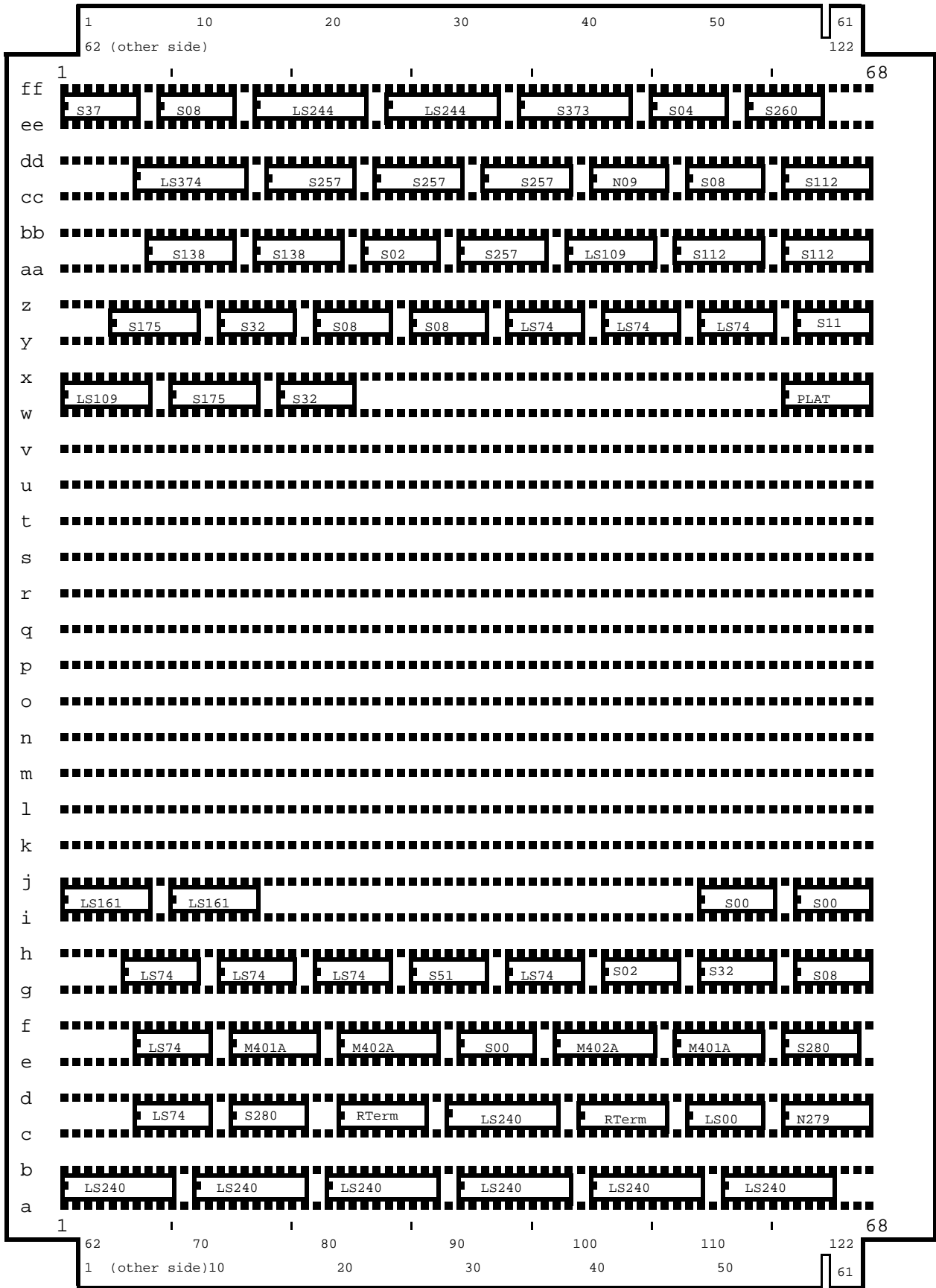
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| XEROX<br>PARC/CSL | Project<br>DDTape | Data Wakeups | File<br>DDTape11.sil | Designer<br>Tim Diebert | Rev<br>E | Date<br>3/17/81 | Page<br>12 |
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1k ohm resistor from 1 to 16  
 330 ohm resistor from 2 to 15

E D G E C O N N E C T O R



C A B L E C O N N E C T O R

Misc Clean up REV D

As viewed from the component side

Load .01uf caps all available locations near chips  
Install heavy ground connections from edge to power p.

|                   |                   |                     |                      |                         |          |                 |            |
|-------------------|-------------------|---------------------|----------------------|-------------------------|----------|-----------------|------------|
| XEROX<br>PARC/CSL | Project<br>DDTape | Reference<br>Layout | File<br>DDTape14.sil | Designer<br>Tim Diebert | Rev<br>E | Date<br>3/17/81 | Page<br>15 |
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