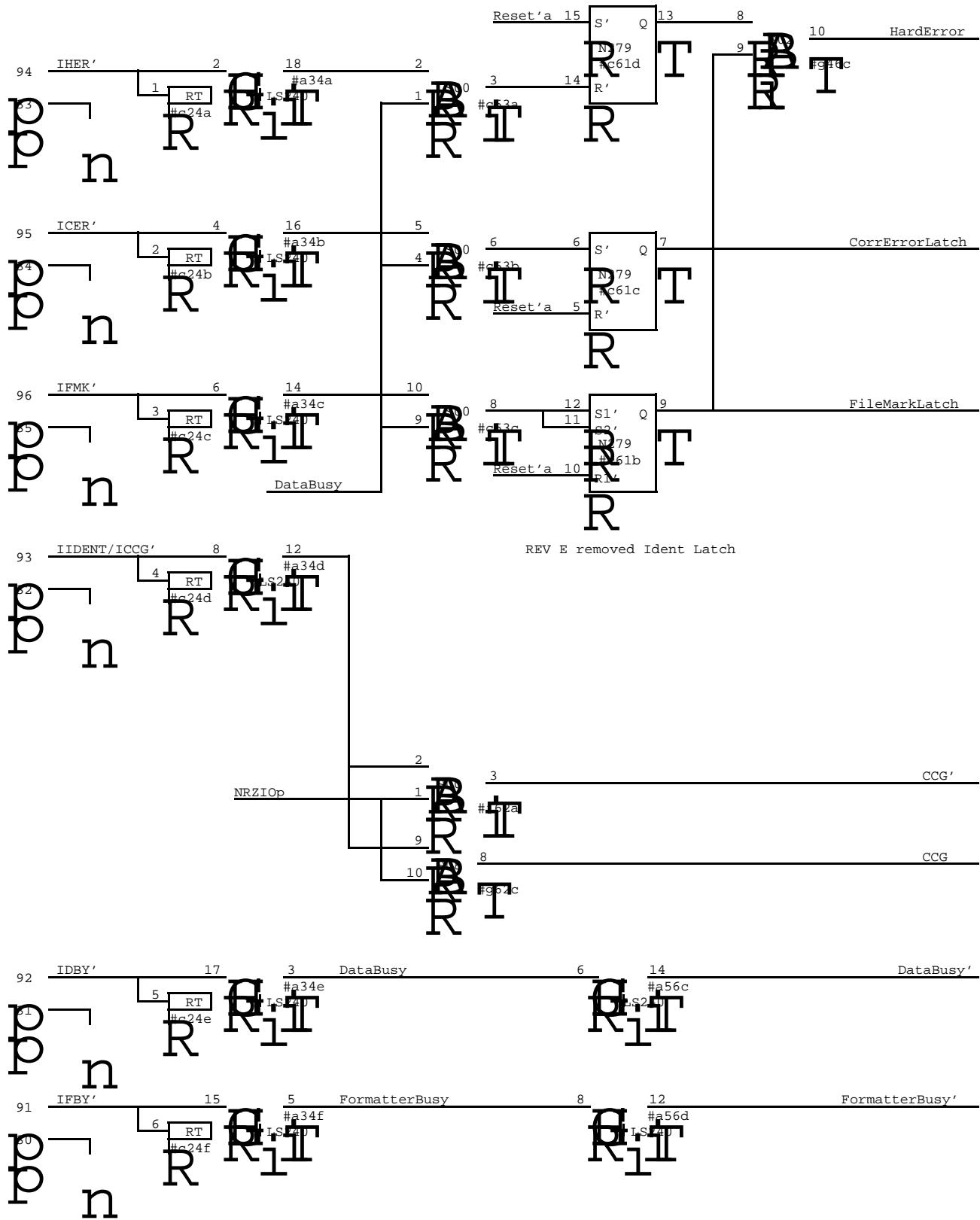
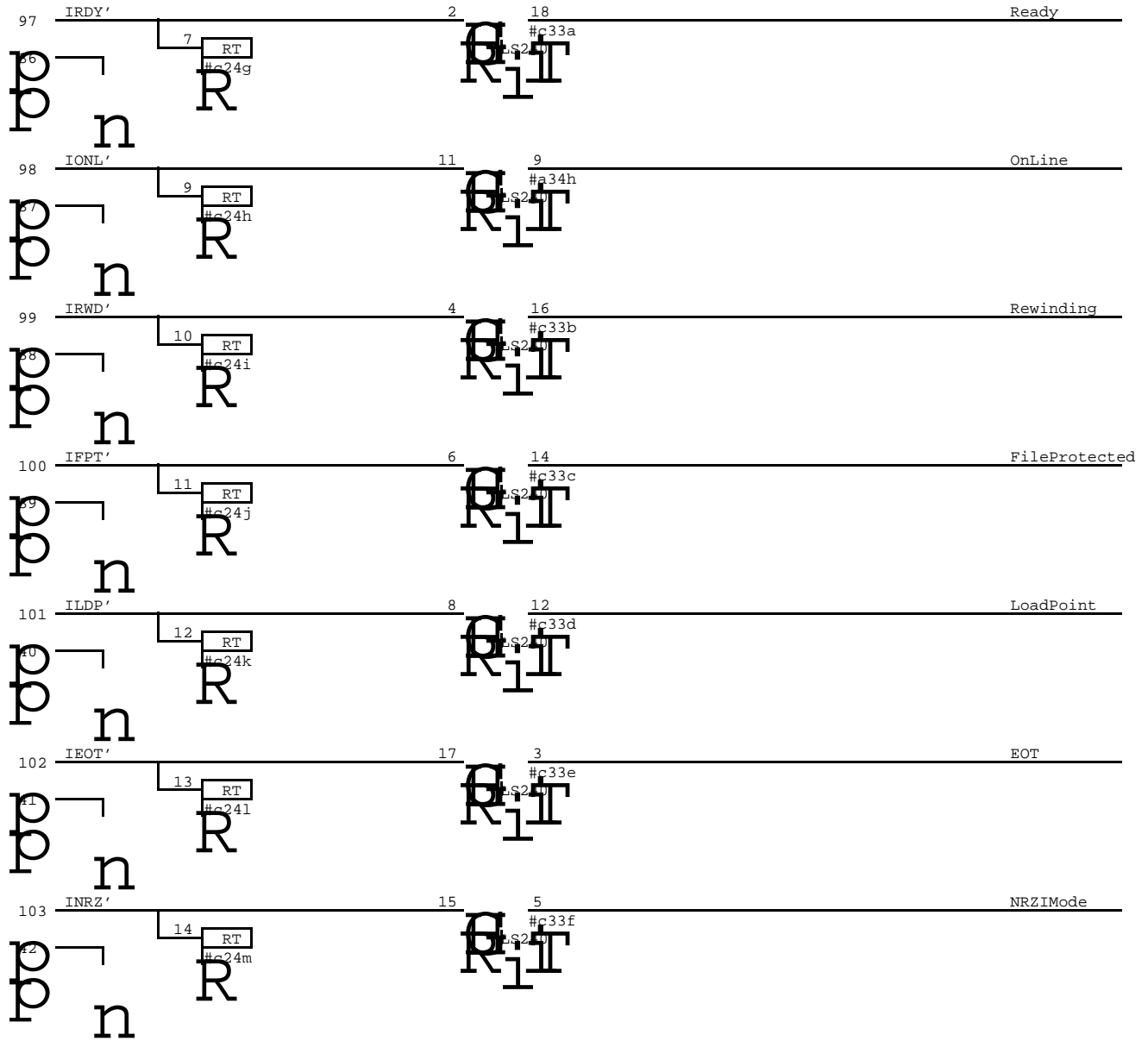


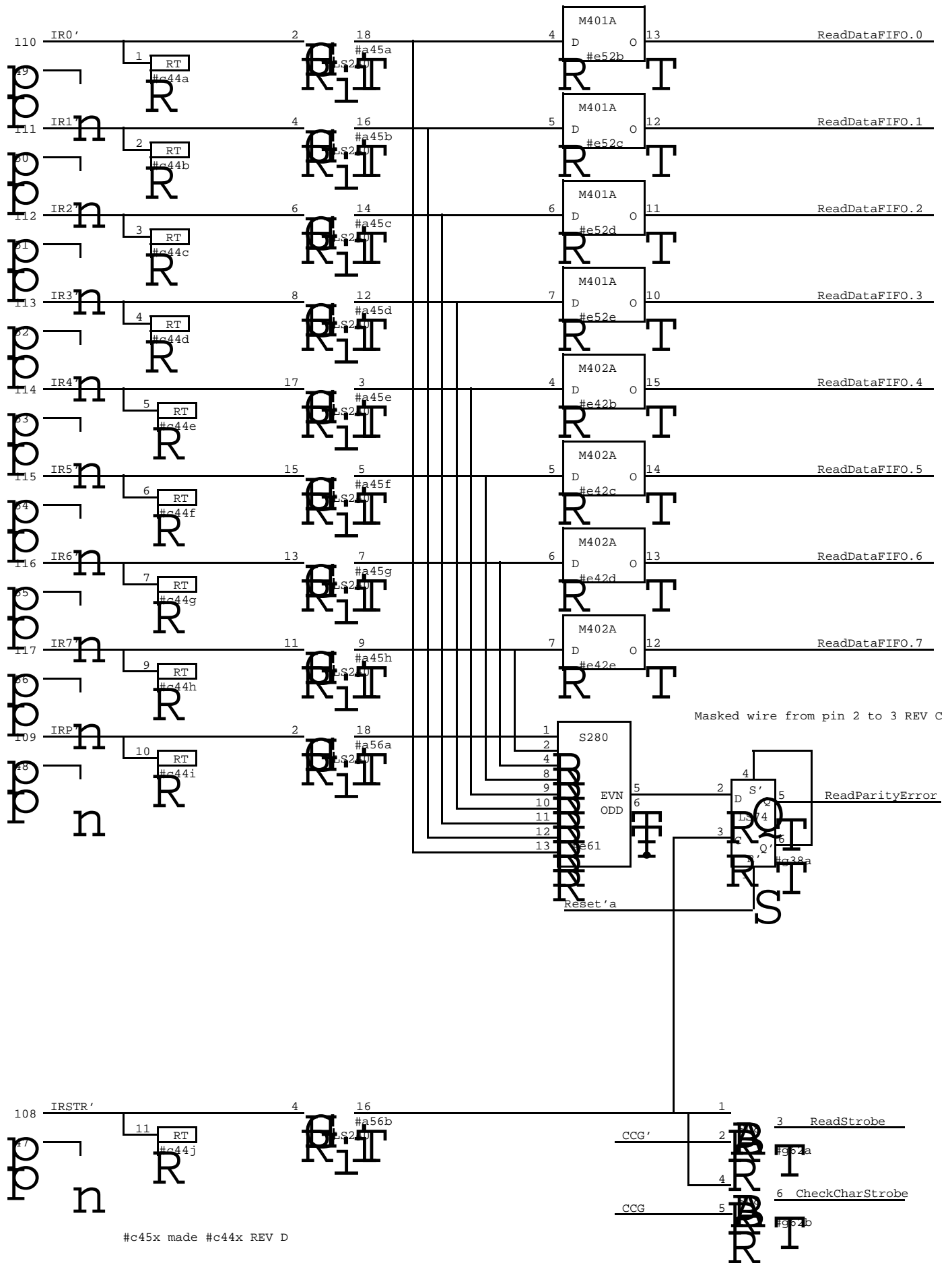
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 T A P E   C O N T R O L L E R  
 D D T a p e

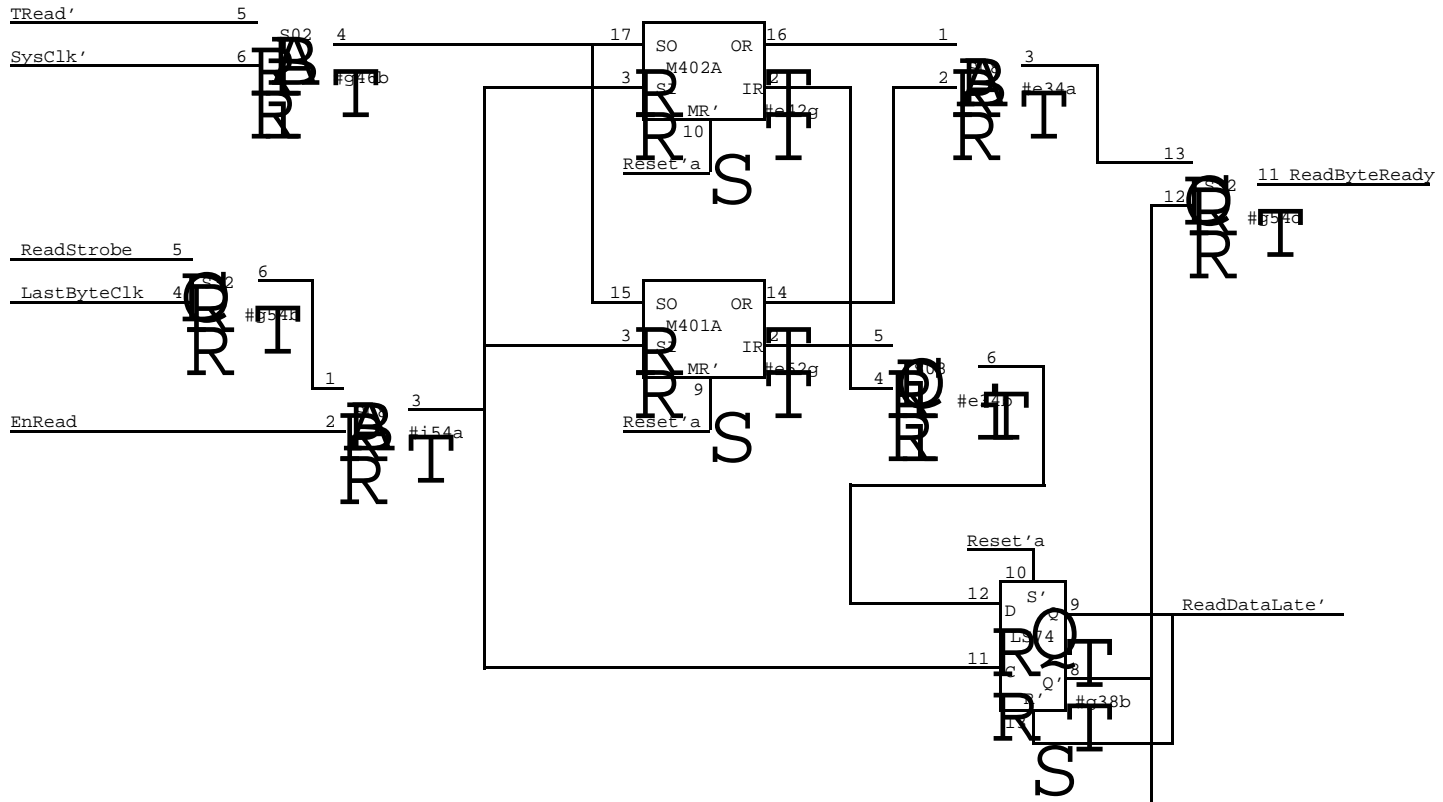
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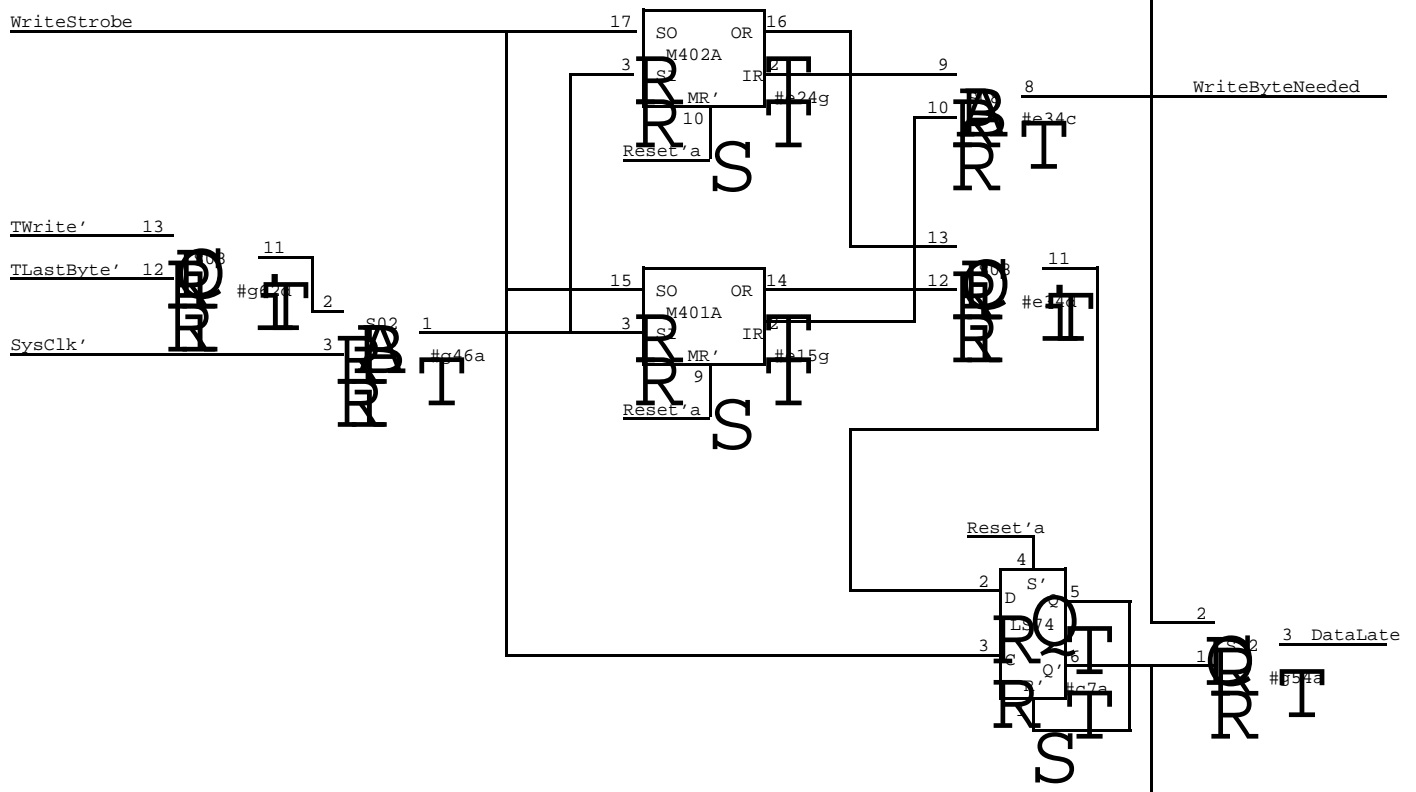




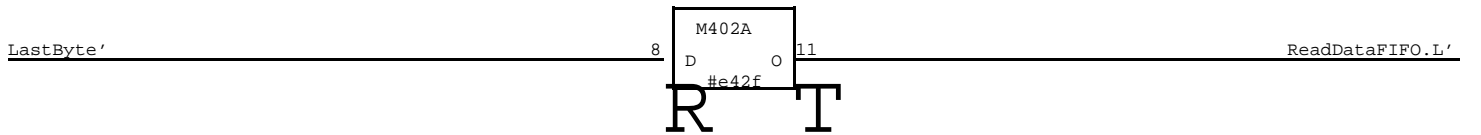
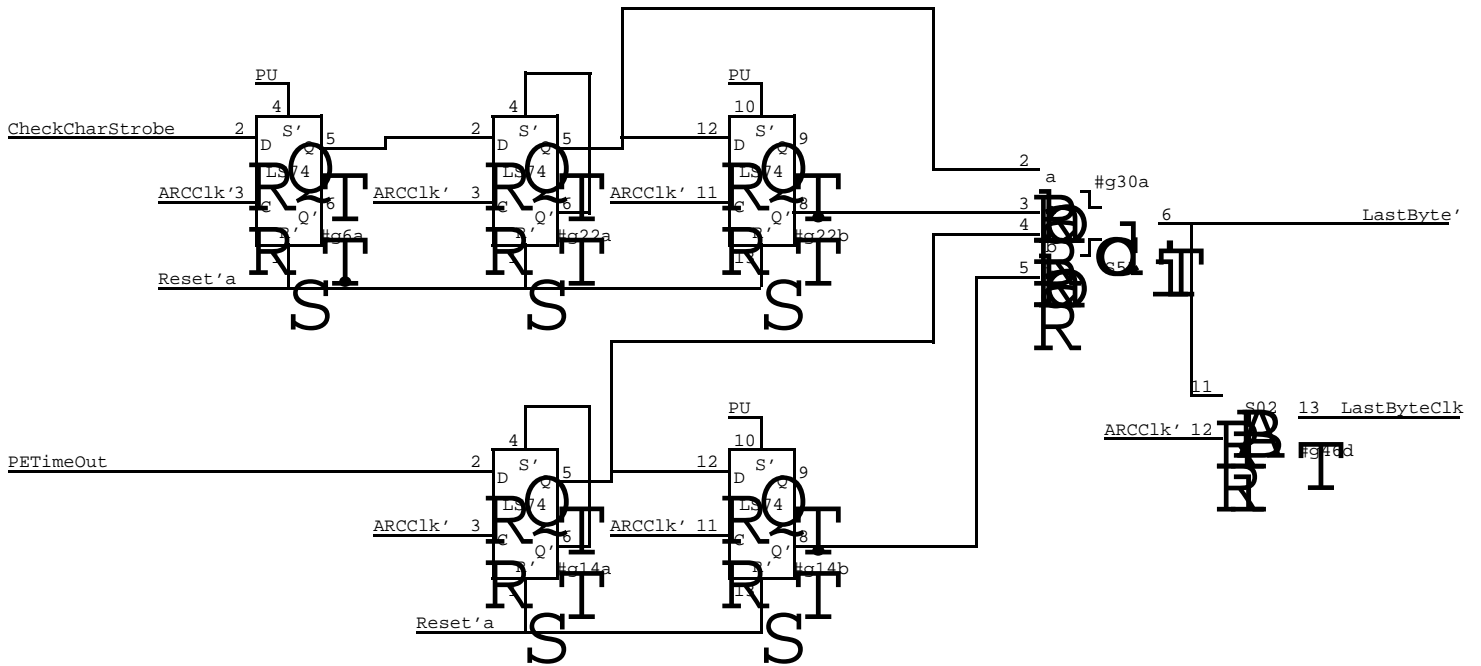
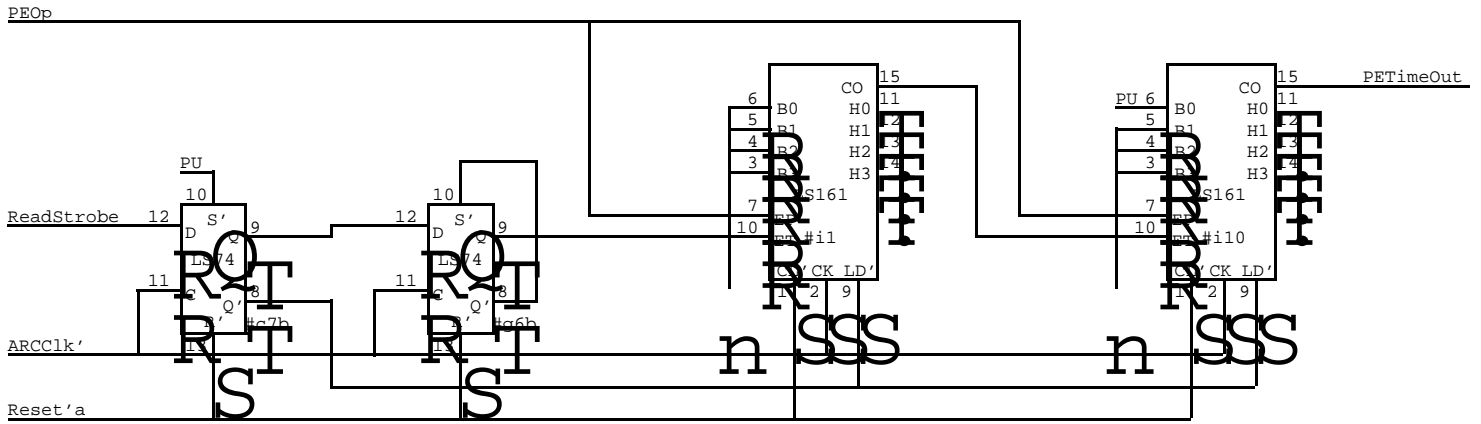


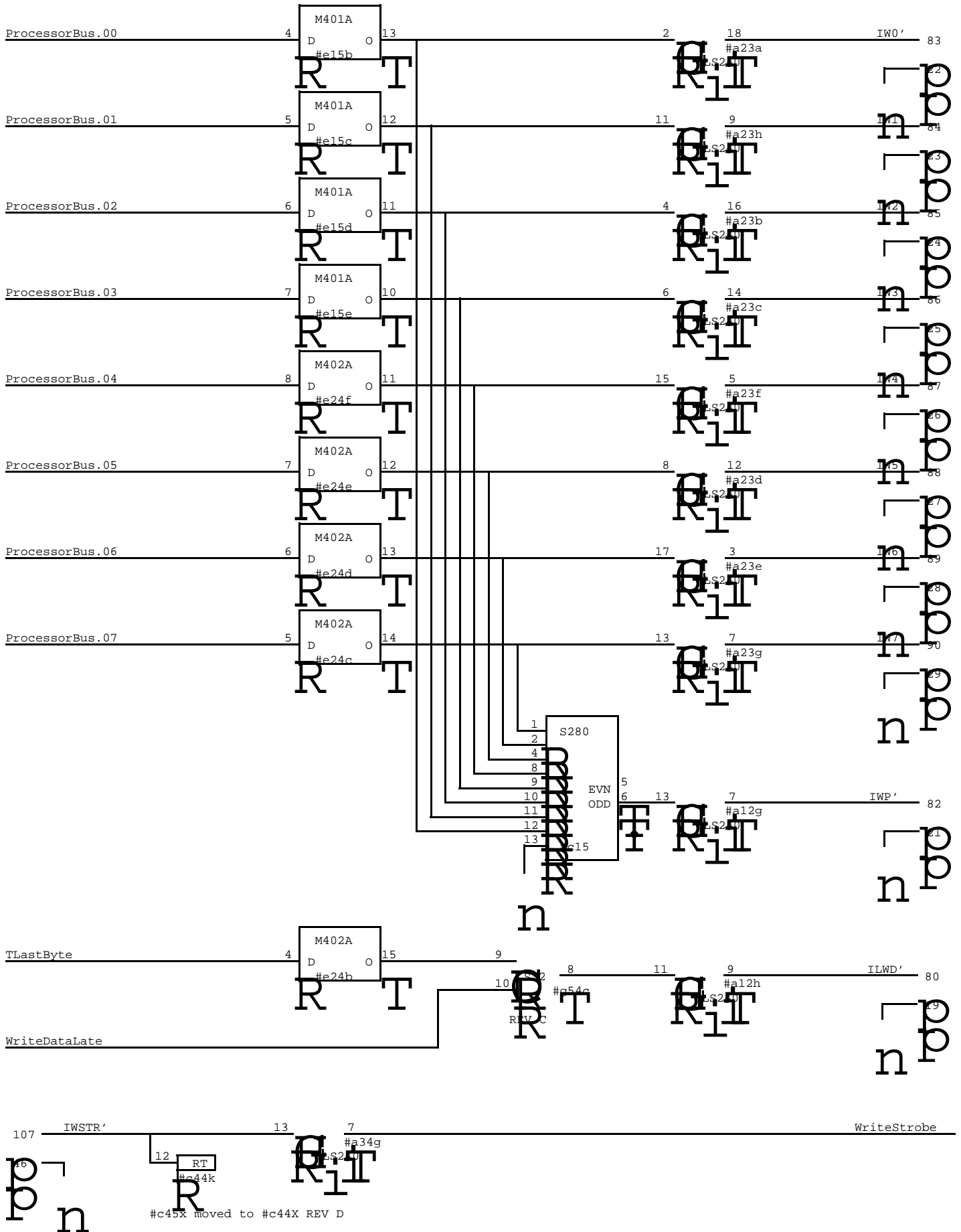


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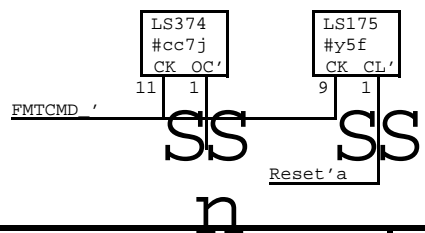
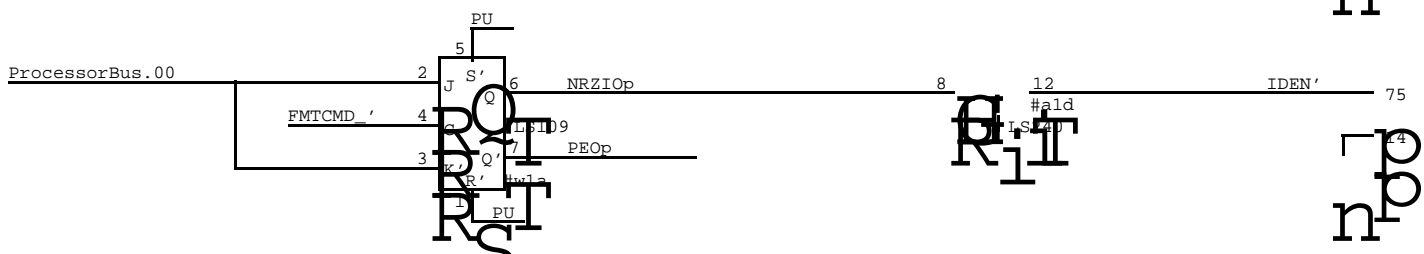
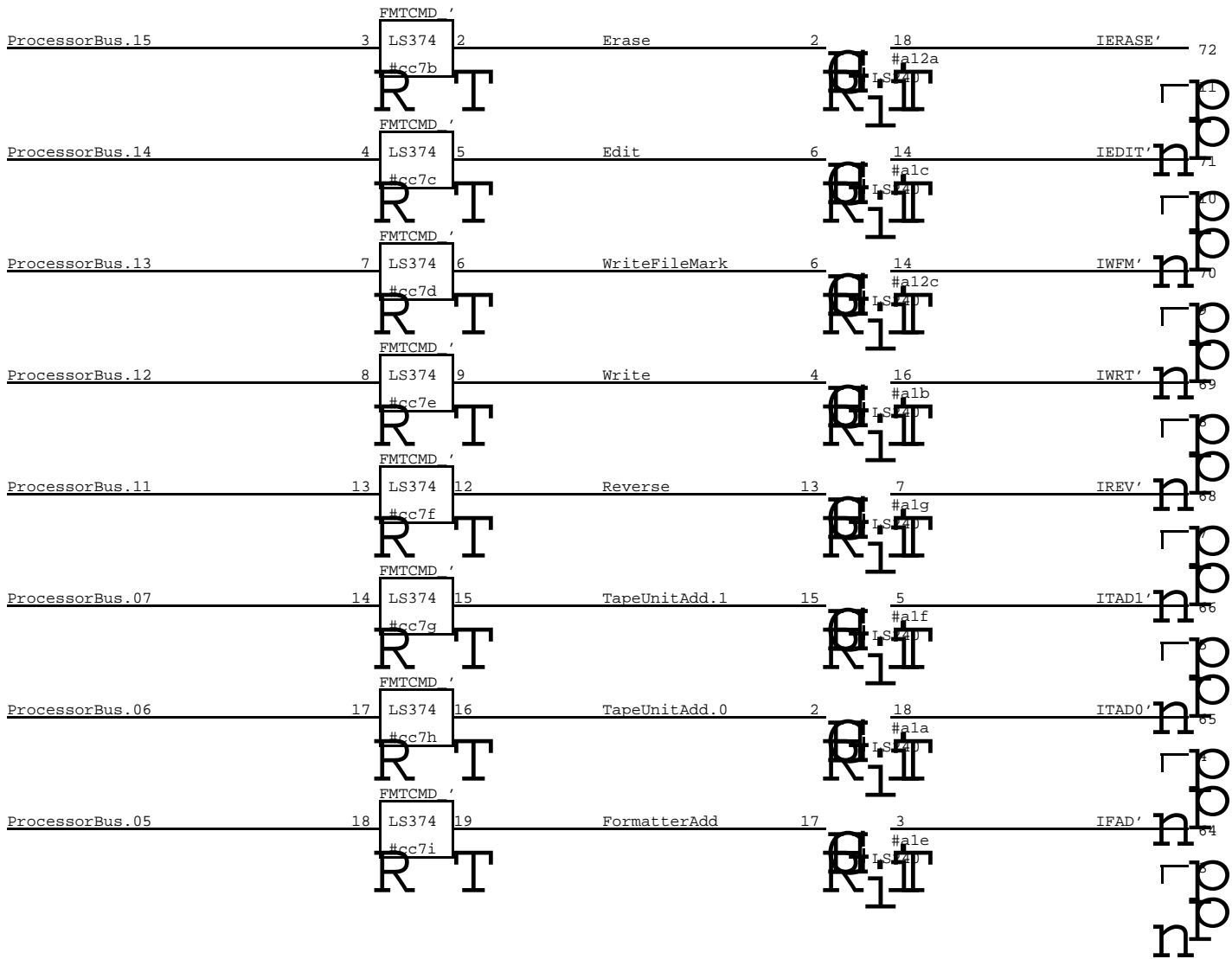


Write FIFO Control

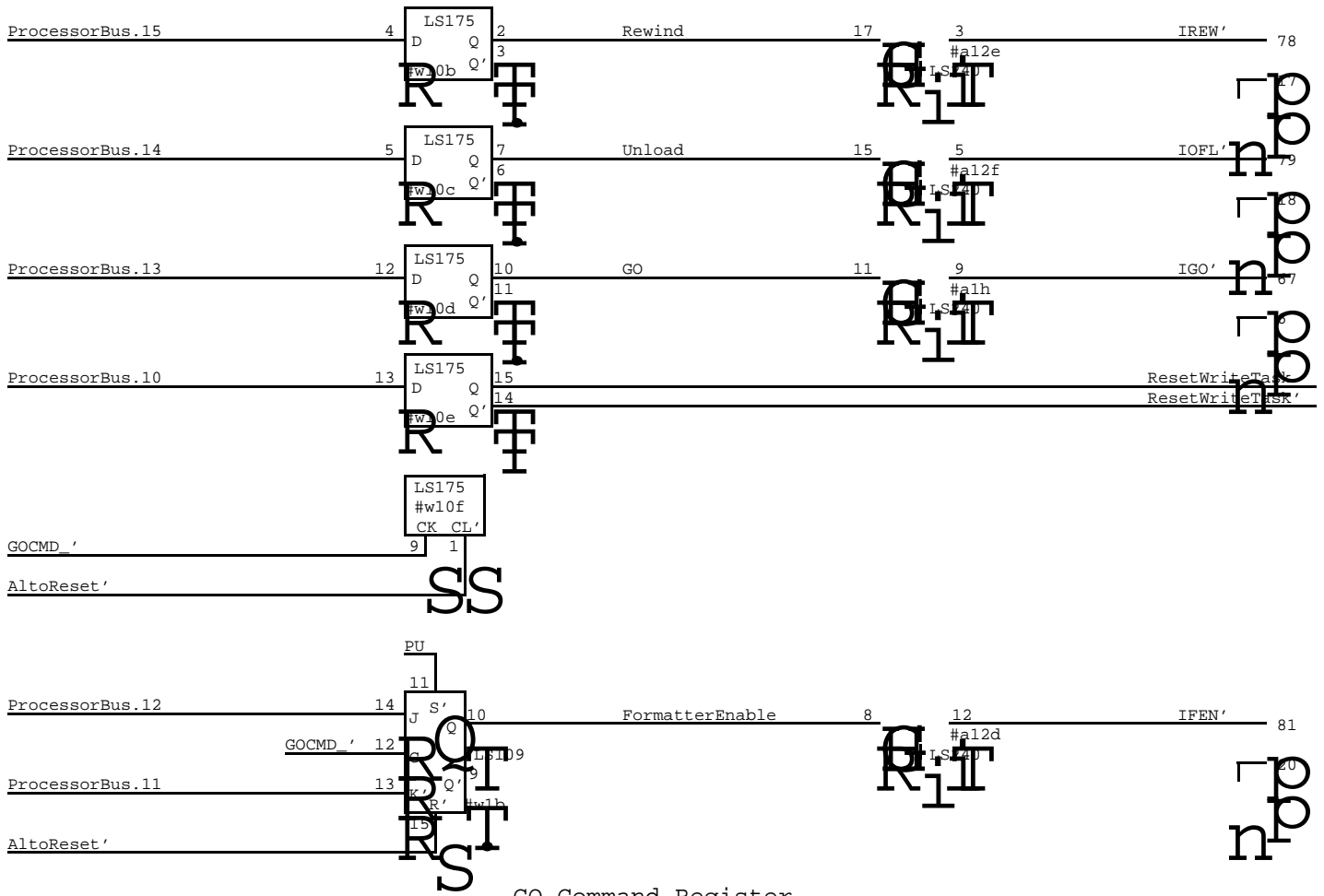




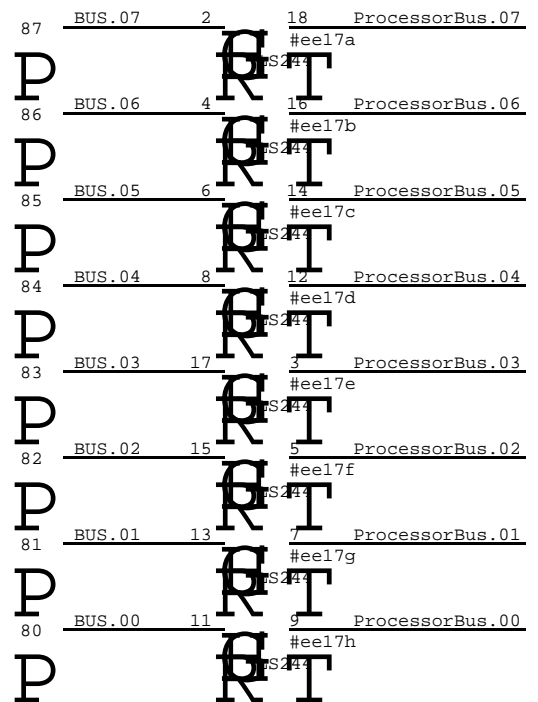
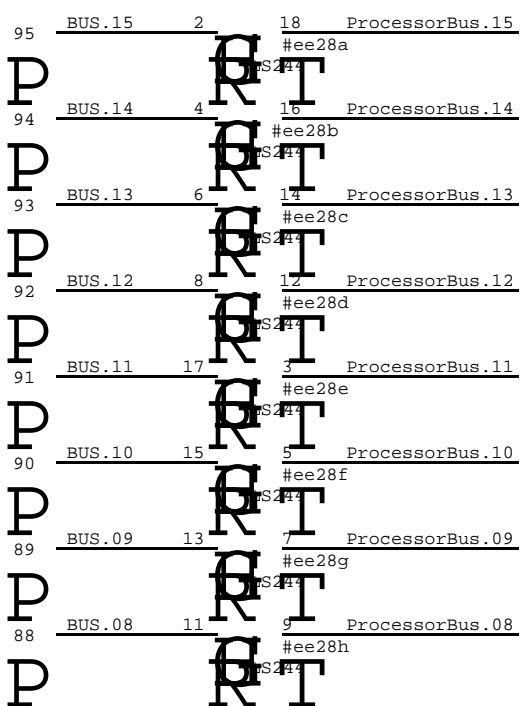
#c45X moved to #c44X REV D





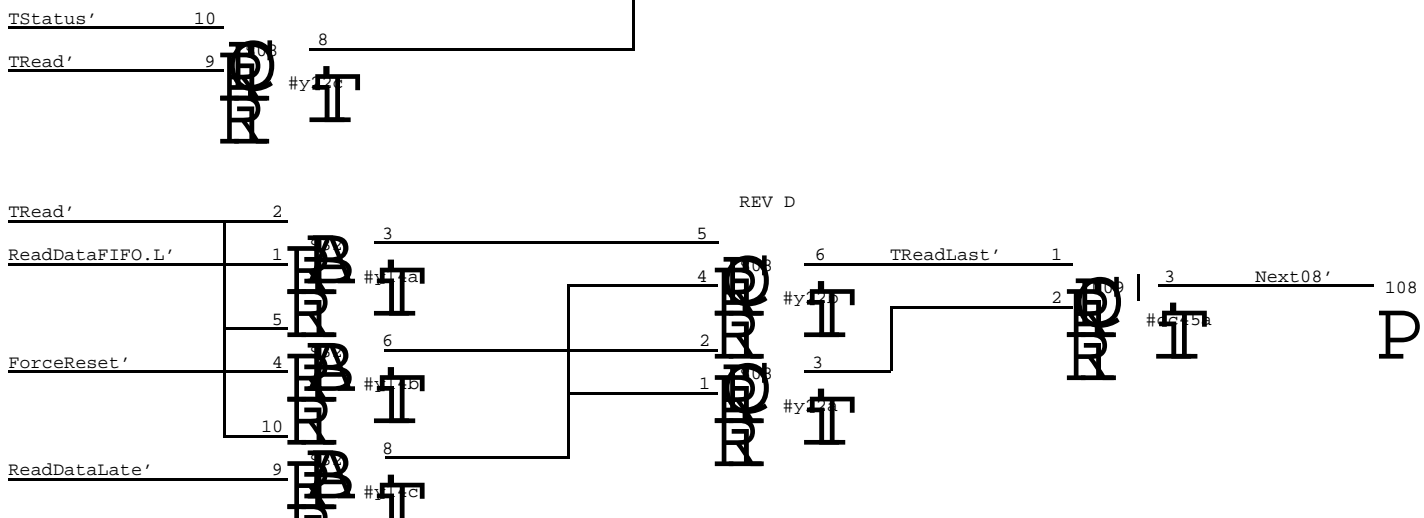
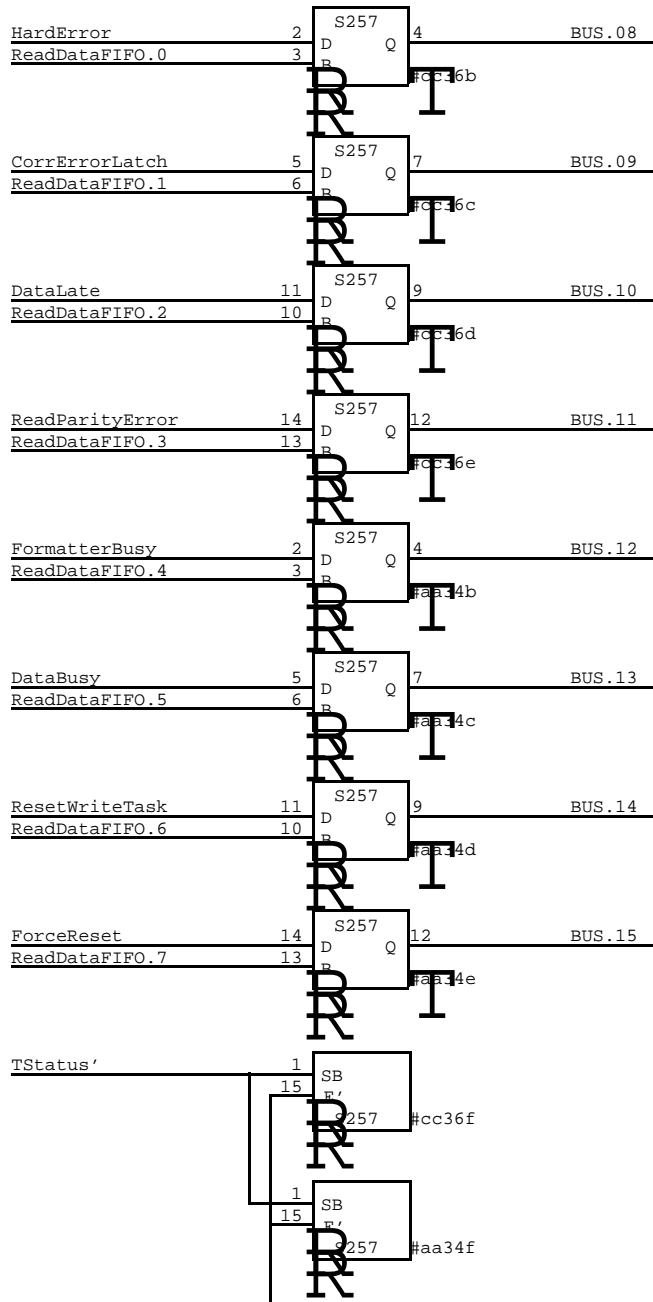
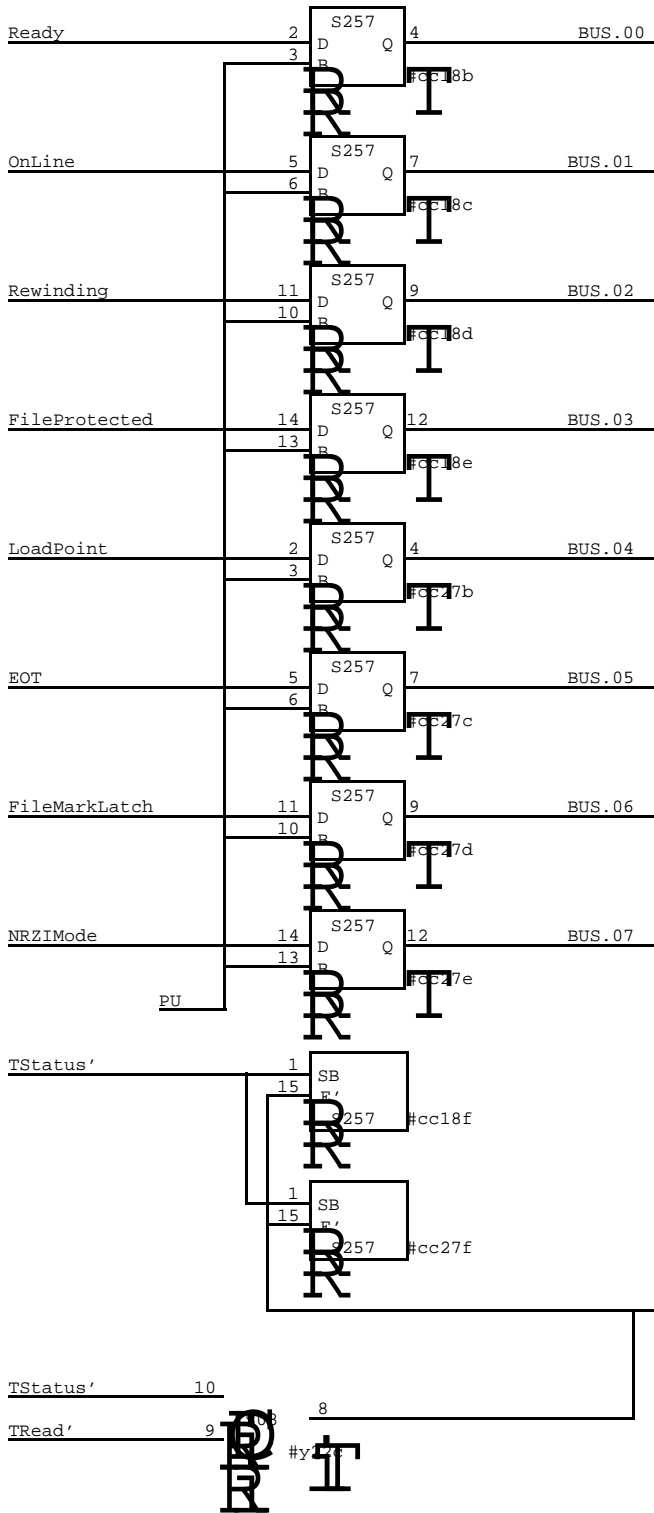


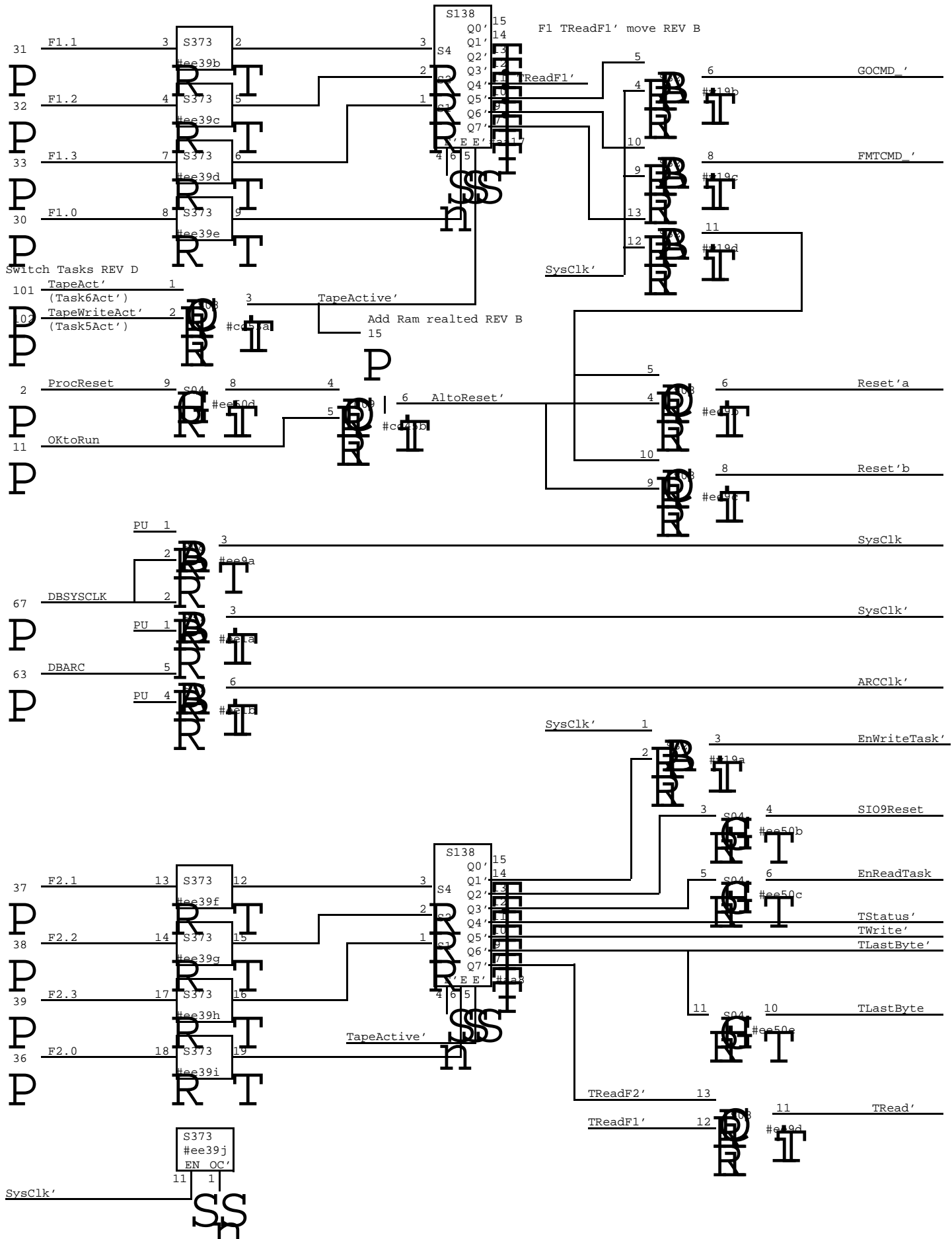
GO Command Register

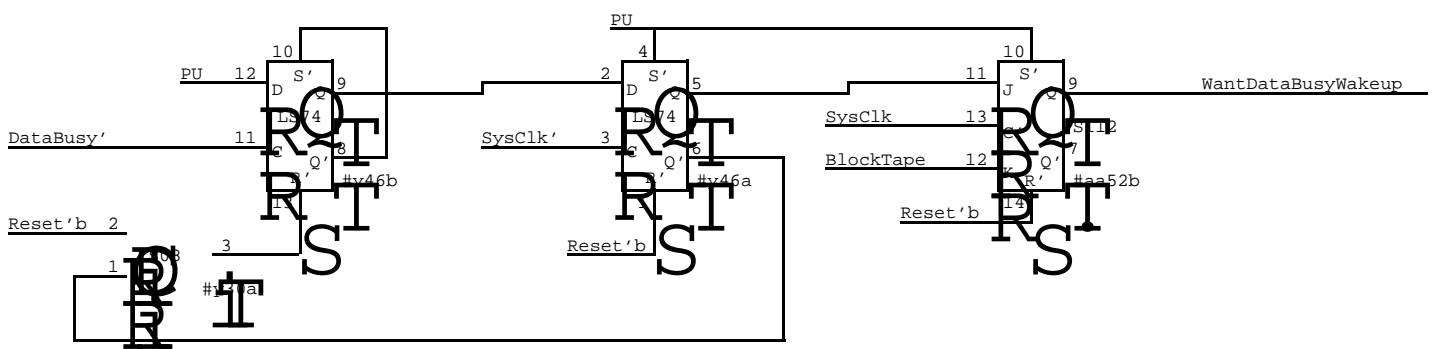
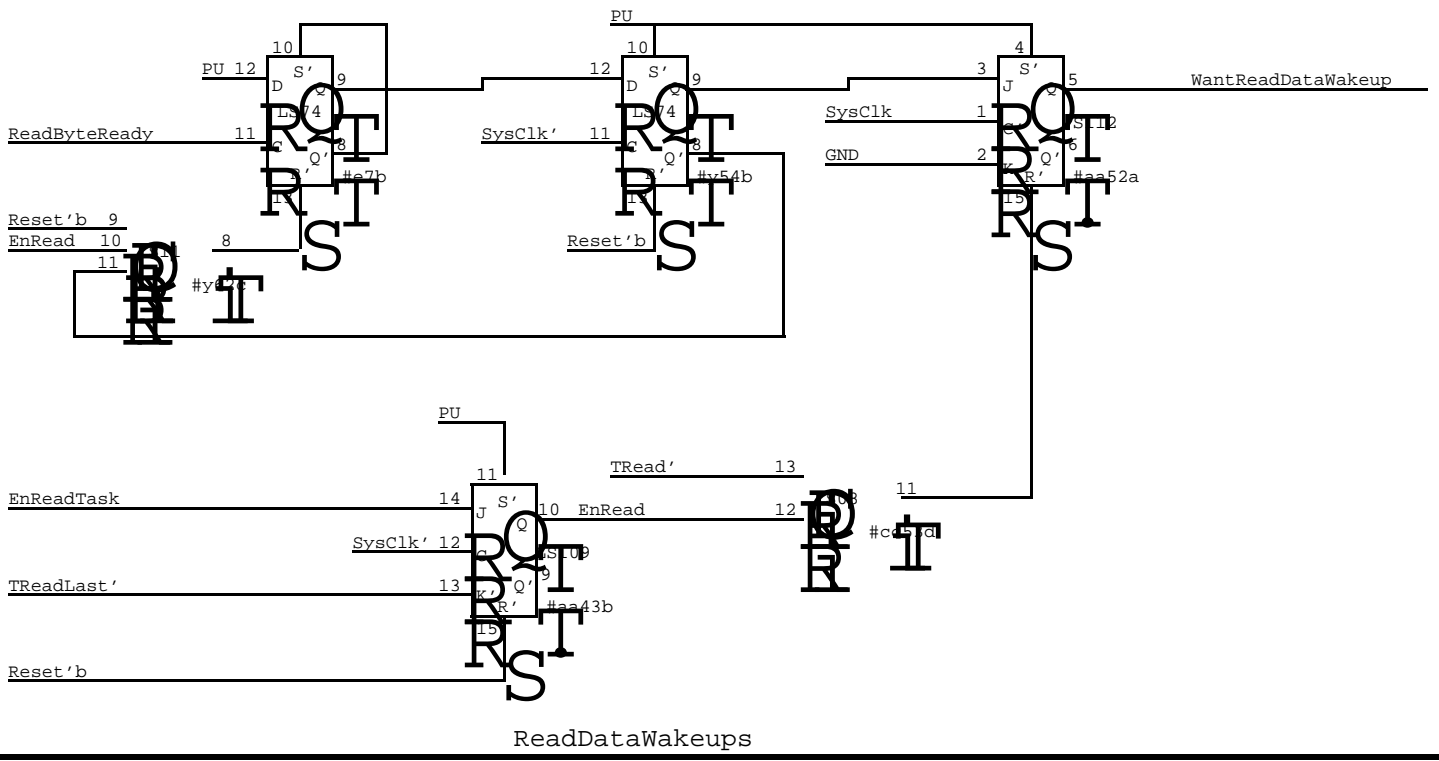
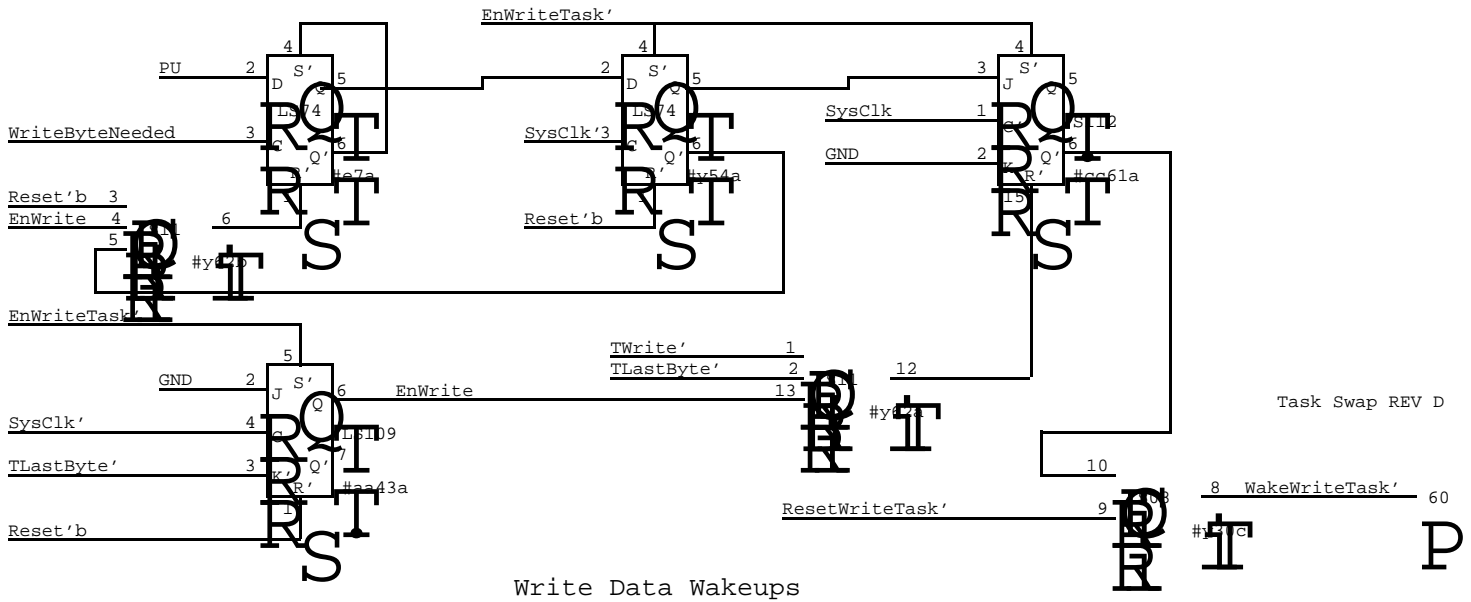


Alto Bus Interface

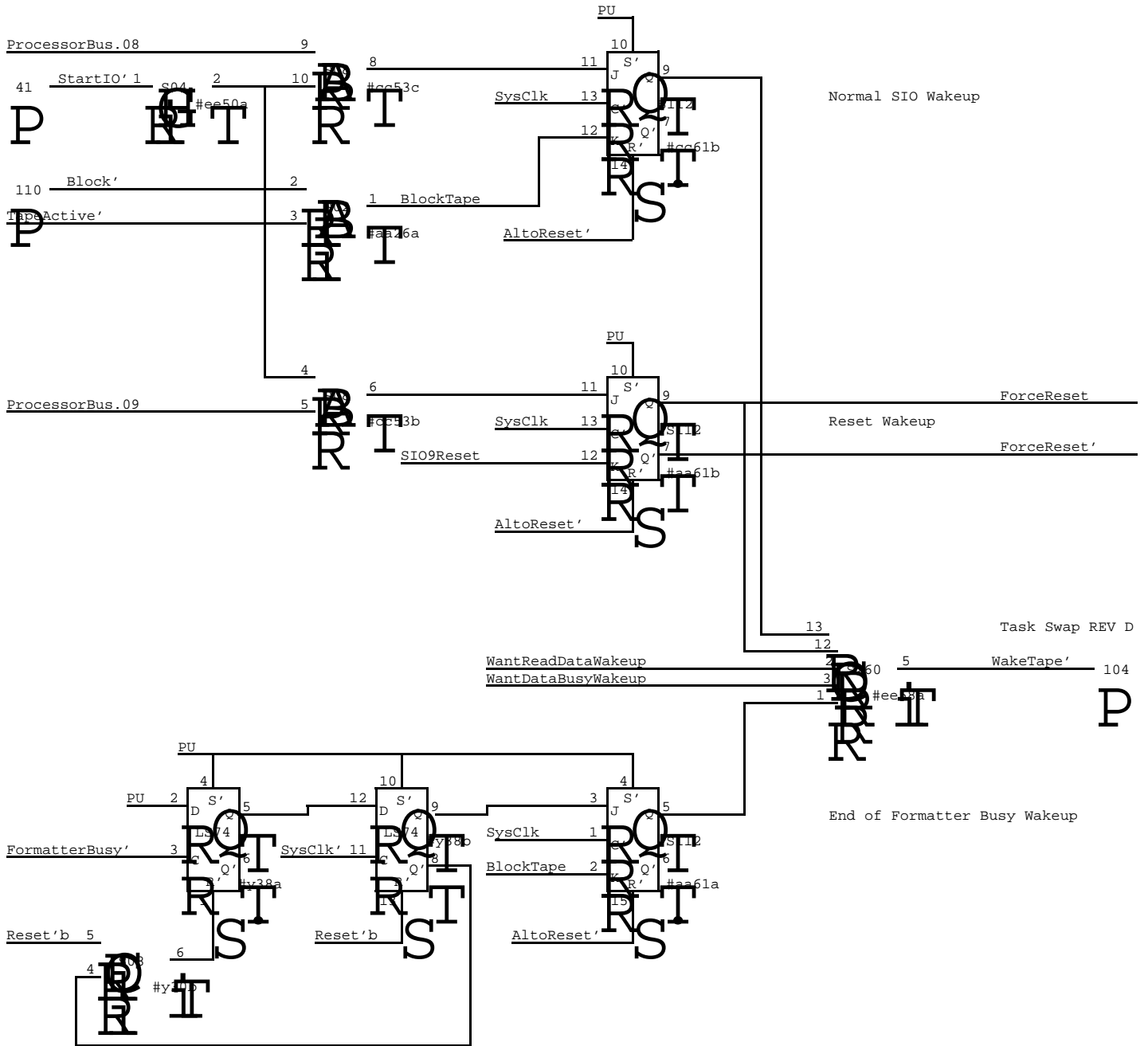
XEROX PARC/CSL	Project DDTape	GO Command Register Alto Bus Interface	File DDTape08.sil	Designer Tim Diebert	Rev F	Date 1/05/82	Page 09
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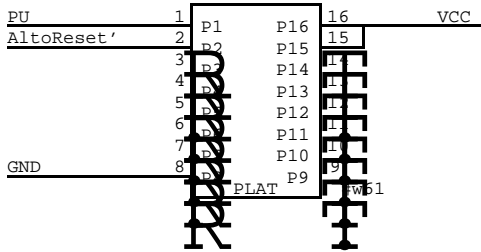
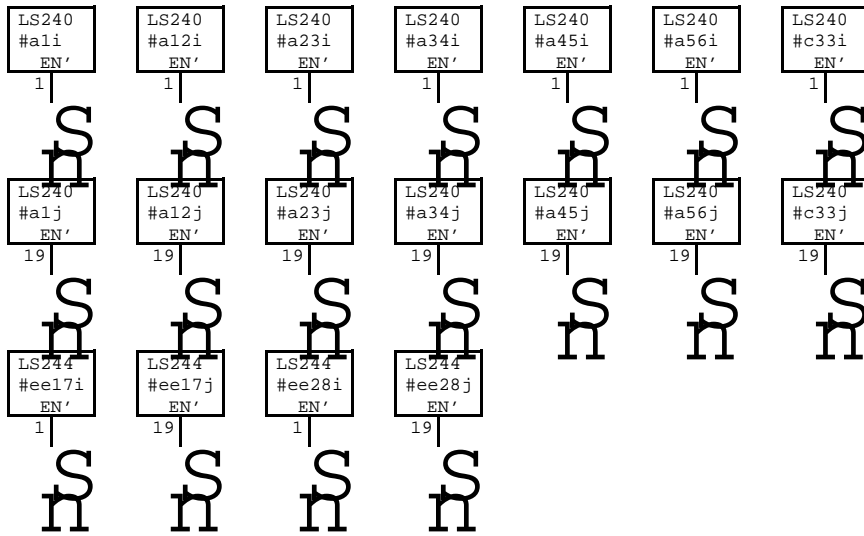






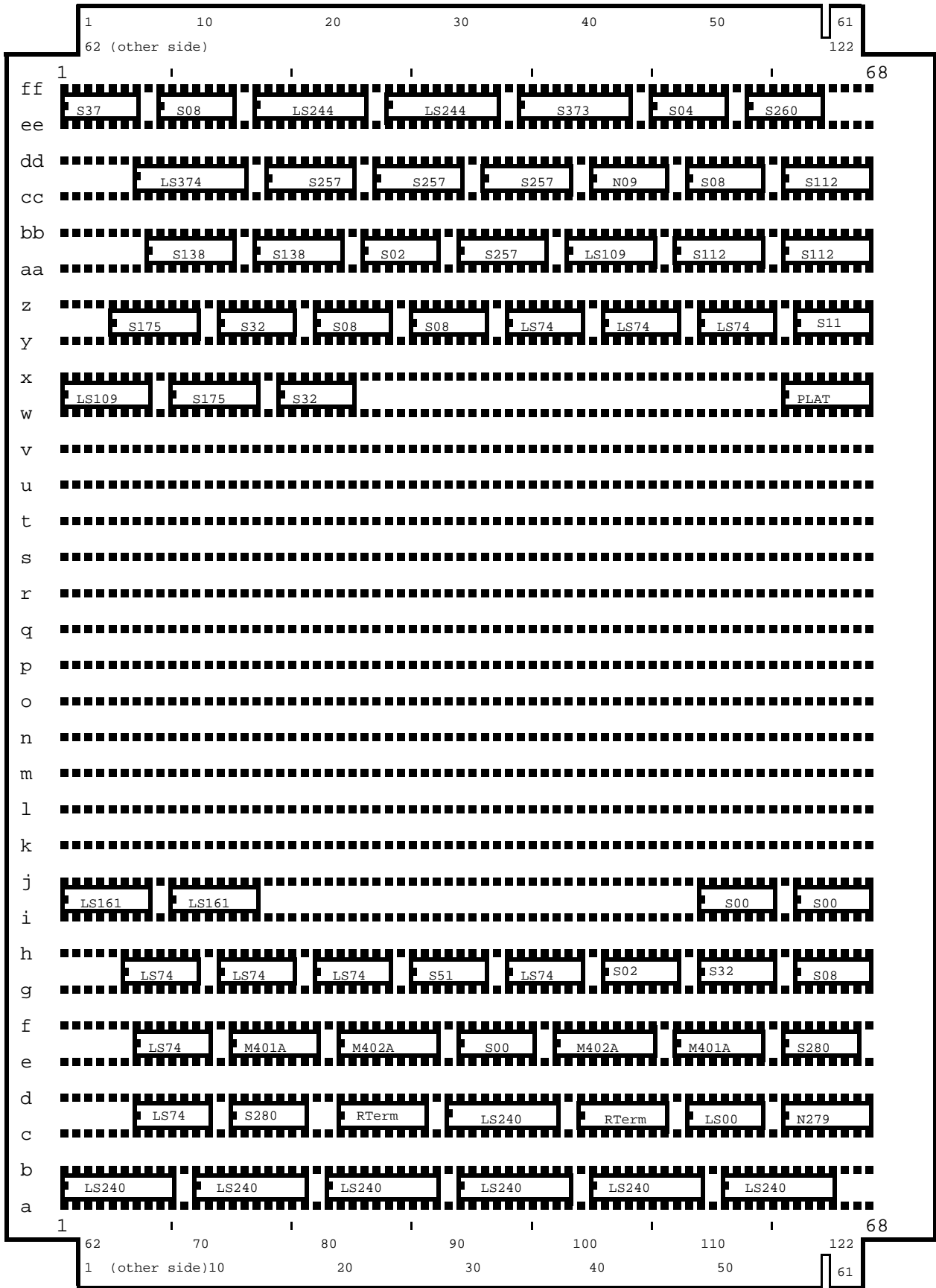
XEROX	Project	File	Designer	Rev	Date	Page
PARC/CSL	DDTape	DDTape11.sil	Tim Diebert	F	3/17/81	12
	Data Wakeups					





1k ohm resistor from 1 to 16  
 330 ohm resistor from 2 to 15

E D G E C O N N E C T O R



C A B L E C O N N E C T O R

Misc Clean up REV D

As viewed from the component side

Load .01uf caps all available locations near chips  
Install heavy ground connections from edge to power p.

XEROX PARC/CSL	Project DDTape	Reference Layout	File DDTape14.sil	Designer Tim Diebert	Rev F	Date 3/17/81	Page 15
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