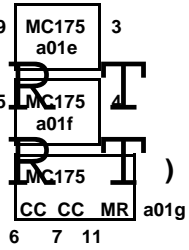
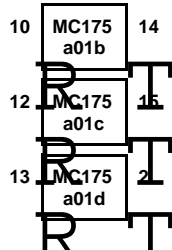
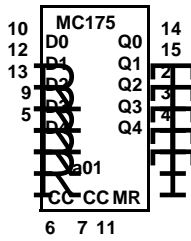


MC175

Quint Latch

(8)

Q (8)



D	CC	CC	MR	Q(n+1)
L	L	L	L	L
H	L	L	L	H
X	H	X	L	Q(n)
X	X	H	L	Q(n)
X	H	X	H	L
X	X	H	H	L

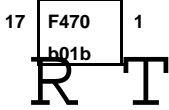
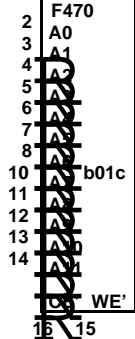
Tpdd = 3.6 (data)
 Tpdc = 4.4 (clock)
 TpdR = 4.2 (reset)
 Ts = 3.7 (setup)
 Th = 2.2 (hold)

F470

4K x 1 random access memory

\$ (8)

Q (8)



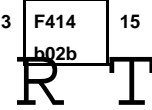
Taad = 35 A access
 Tace = 15 CE access
 Tw' = 25 write pulse
 Tsd = 5 setup data
 Thd = 5 hold data
 Tsa = 10 setup addr
 Tha = 5 hold addr
 Tsce = 5 setup CE
 Thce = 5 hold CE
 Twd = 15 write disable
 Twr = 20 write recover
 Tcer = 15 CE recover

F414

256 x 1 random access memory

~ (8)

Q (8)



Taad = 10 A access
 Tace = 6 CE access
 Tw' = 7 write pulse
 Tsd = 1 setup data
 Thd = 2 hold data
 Tsa = 1 setup addr
 Tha = 2 hold addr
 Tsce = 1 setup CE
 Thce = 2 hold CE
 Twd = 8 write disable
 Twr = 10 write recover
 Tcer = 6 CE recover

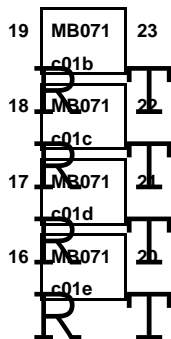
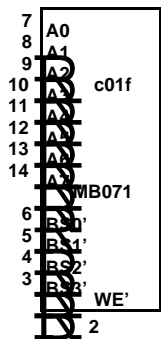
MB071

256 x 4 random access memory

QIT package + platform

% (8)

Q (8)



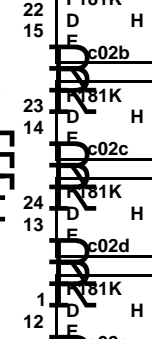
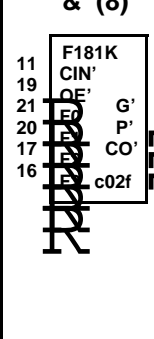
Taad = 10.0 A access
 Tabs = 4.5 BS access
 Tw' = 8.0 write pulse
 Tsd = 2.0 setup data
 Thd = 2.0 hold data
 Tsa = 2.0 setup addr
 Tha = 2.0 hold addr
 Tsbs = 2.0 setup BS
 Thbs = 2.0 hold BS
 Twd = 5.0 write disable
 Twr = 9.0 write recover
 Tbsr = 4.5 BS recover

F181K

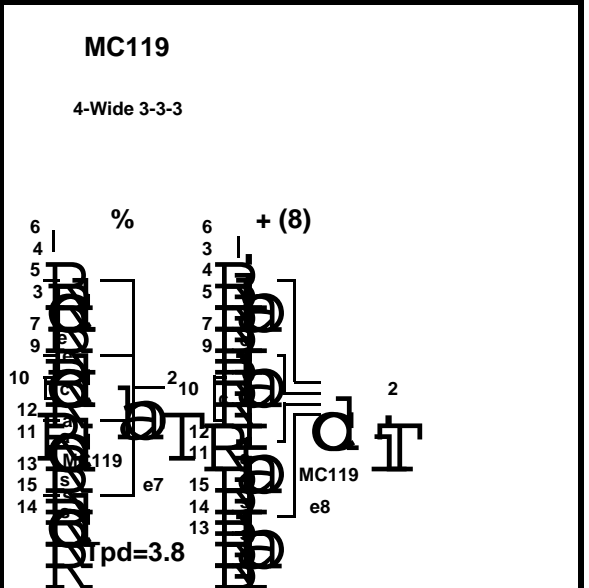
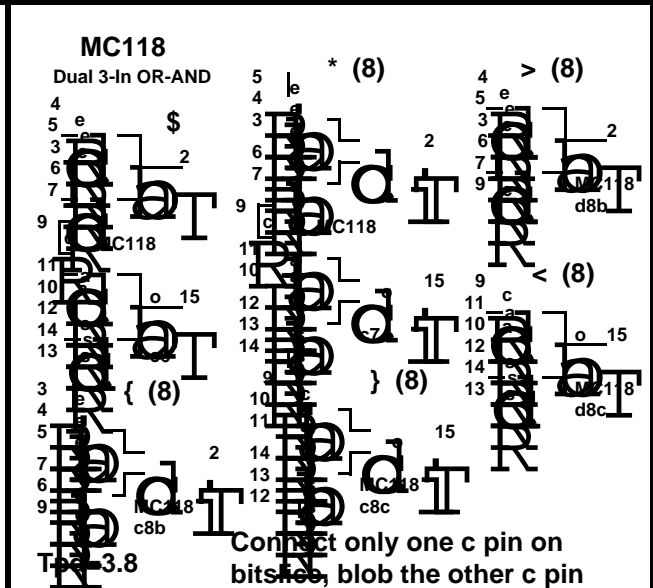
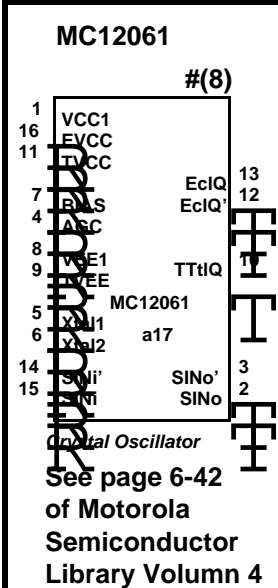
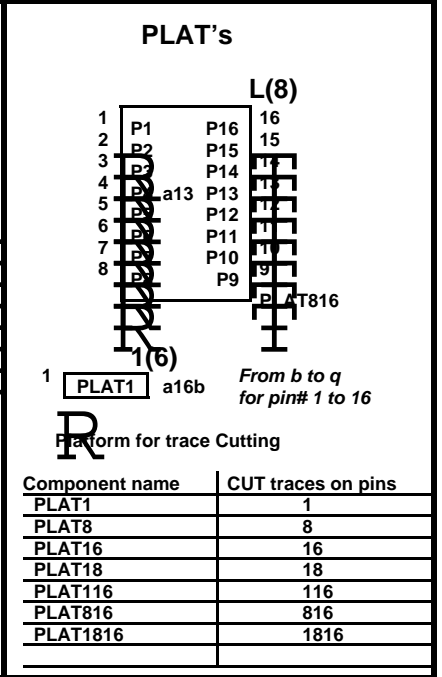
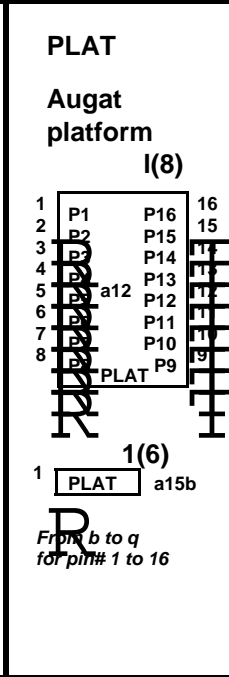
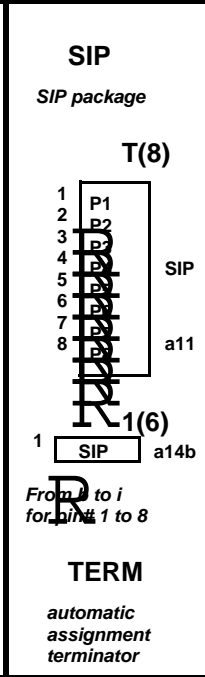
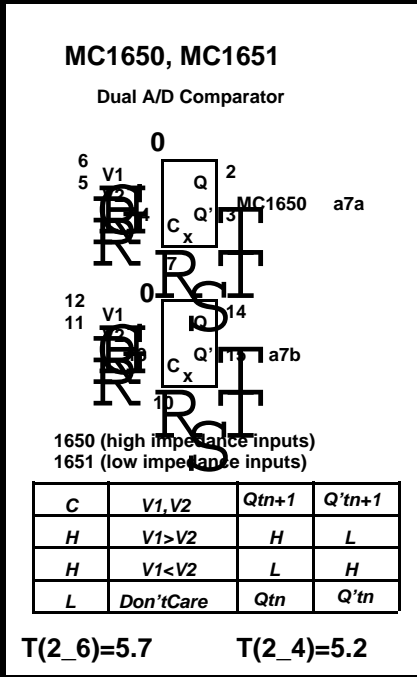
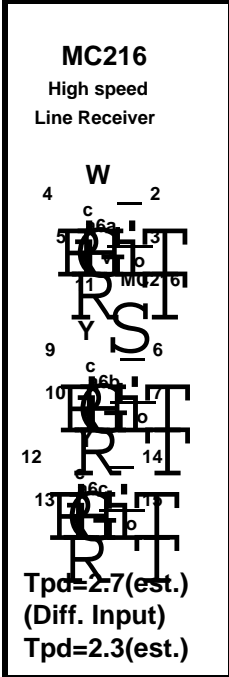
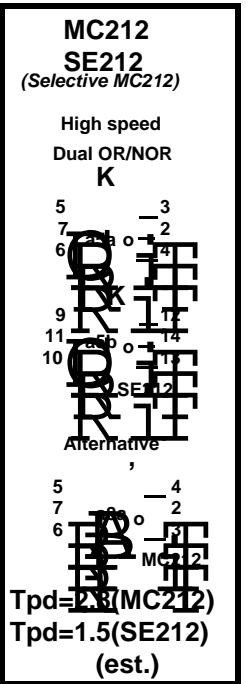
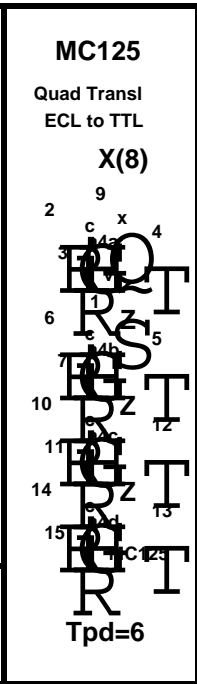
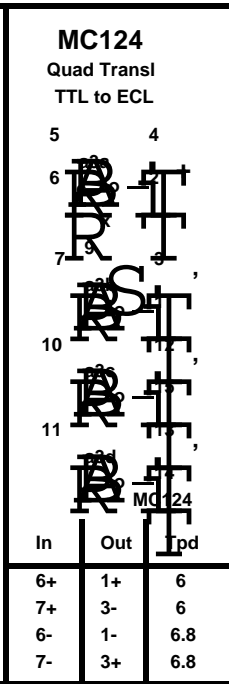
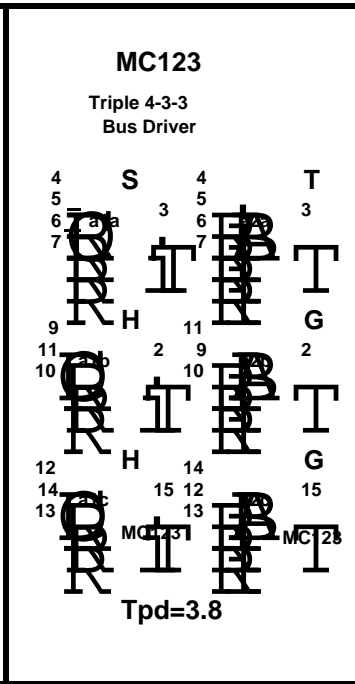
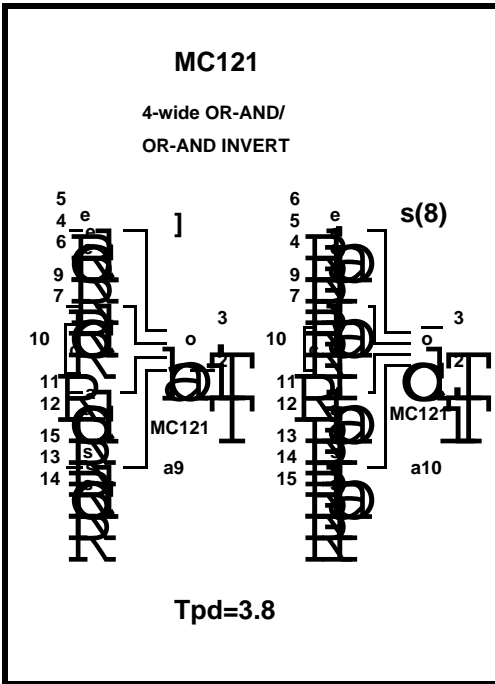
*100K series 4 bit ALU
 0.4 wide DIP package*

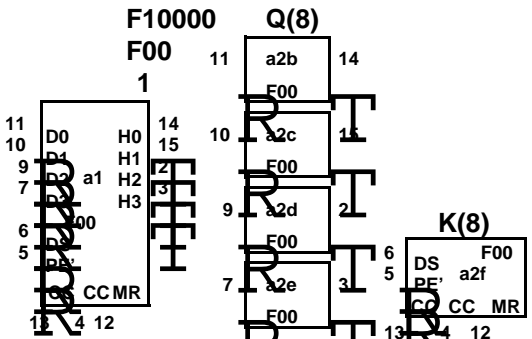
& (8)

2 (8)



Tdh = 6.5 D to H
 Teh = 6.5 E to H
 Tfh = 6.5 F to H
 TcinH = 4.7 CIN to H
 Tcio = 3.6 CIN to CO
 Tdpg = 4.1 D to P,G
 Tepg = 4.1 E to P,G
 TfpG = 4.1 F to P,G
 Tdco = 5.4 D to CO
 Teco = 5.4 E to CO
 Tfco = 5.4 F to CO
 Toeh = 2.1 OE to H

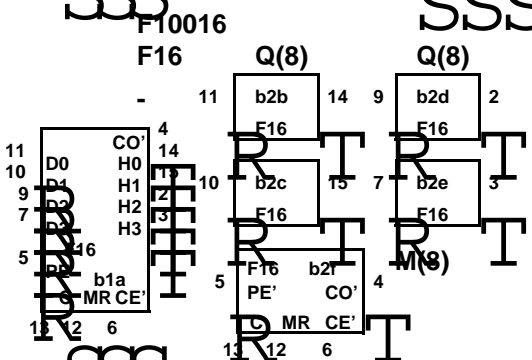




4 bit Shift Register

MR	PE'	CC	MODE	FUNCTION
H	X	X	X	reset - all outputs low
L	L	L	^^	parallel load
L	L	^^	L	parallel load
L	H	^^	L	shift left
L	H	L	^^	shift left
L	X	H	X	hold
L	X	X	H	hold

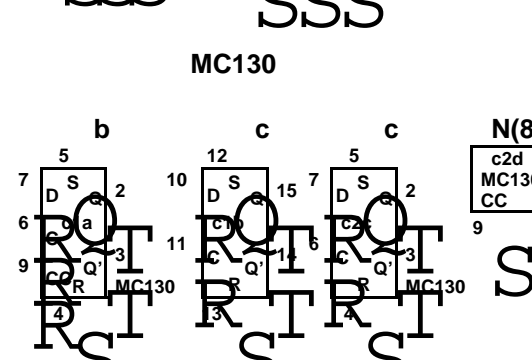
Tpd=5.5
 Tw'=3.8 (clock pulse width)
 Ts =1.7 (data setup)
 Th =1.1 (data hold)
 Tse=6.0 (PE' setup)
 (all times estimates)



4 bit Binary Counter

CE'	PE'	MR	CP	FUNCTION
L	L	L	^^	parallel load
H	L	L	^^	parallel load
L	H	L	^^	count
H	H	L	^^	hold
X	X	L	/	masters open, slaves hold
X	X	H	X	reset

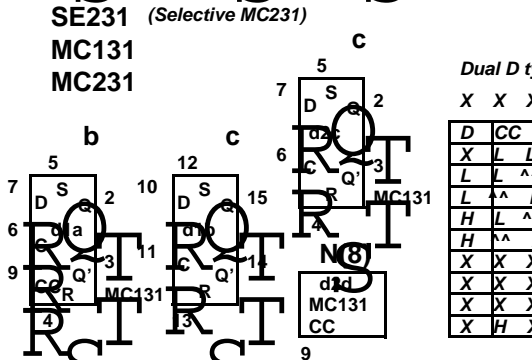
Tpd=5.5
 Tw =3.5 (clock pulse width)
 Ts =2.2 (data setup)
 Th =1.1 (data hold)
 Tse=2.8 (PE' and CE' setup)



Dual Latch

D	CC	C	S	R	Qn+1	FUNCTION
L	L	L	X	X	L	Q follows D
H	L	L	X	X	H	Q follows D
X	X	X	L	L	Qn	hold
X	X	H	L	L	Qn	hold
X	H	X	H	L	H	set
X	X	H	H	L	H	set
X	H	X	L	H	L	reset
X	X	H	L	H	L	reset
X	H	X	H	H		indeterminate

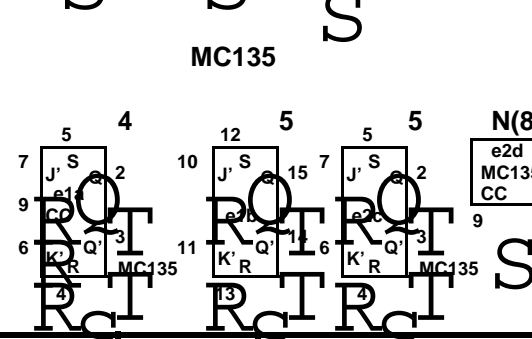
obsolete: MC130
 Tpd=4.1
 Ts =2.8 est
 Th =1.7 est



Dual D type Master-Slave Flip-flop

D	CC	C	S	R	Qn+1	FUNCTION
X	L	L	L	L	Qn	hold
L	L	^^	L	L	L	memory
L	^^	L	L	L	L	memory
H	L	^^	L	L	H	memory
H	^^	L	L	L	H	memory
X	X	X	H	L	H	set
X	X	X	L	H	L	reset
X	X	X	H	H		indeterminate
X	H	X	H	H		indeterminate

obsolete: MC131
 MC131 Tpd=5.0
 MC231 Tpd=3.7
 SE231 Tpd=2.5
 Ts =2.8
 Ts =1.1
 Ts =1.1
 Th =1.7
 Th =0.8
 Th =0.8
 (all times estimates)



Dual J-K Master Slave Flip-Flop

RS Truth Table

R	S	Qn+1
L	L	Qn
L	H	H
H	L	L
H	H	indet

Clocked JK Truth Table

J'	K'	Qn+1
L	L	Qn'
H	L	H
L	H	L
H	H	Qn

obsolete: MC135
 Tpd=4.6
 Trs=5.2 (R, S to Q)
 Ts =2.8 est
 Th =1.7 est
 clock= ^^ on CC

MC136 Hexadecimal Counter

Inputs assumed to vary in sequence from top to bottom

SU'	SD'	B0	B1	B2	B3	CI'	C	H0	H1	H2	H3	CO'	Load
L	L	H	H	L	L	X	^^	H	H	L	L	L	L
L	H	X	X	X	X	L	^^	H	H	L	H	H	Count Up
L	H	X	X	X	X	L	^^	H	H	H	H	L	H
L	H	X	X	X	X	L	^^	H	H	H	H	L	Count Up
L	H	X	X	X	X	H	^^	L	H	H	H	H	Hold
H	H	X	X	X	X	X	^^	H	H	H	H	H	Hold
L	L	L	L	H	H	X	^^	L	L	H	H	L	Load
H	L	X	X	X	X	L	^^	L	L	H	L	H	Count Down
H	L	X	X	X	X	L	^^	L	L	L	L	H	Count Down
H	L	X	X	X	X	L	^^	L	L	L	L	L	Count Down
H	L	X	X	X	X	L	^^	H	H	H	H	H	Count Down

TPD=11.5
TSD=3.9 (data setup)
TSS=8.3 (select setup)
TSC=4.1 (CI' setup)
THC=3.4 (CI' ld)
 (all times estimates)

MC141 4 bit Shift Register

SR'	SL'	MODE	Qi(n+1)
L	L	parallel load	Di(n)
L	H	shift right	Qi-1(n)
H	L	shift left	Qi+1(n)
H	H	hold	Qi(n)

TPD=4.2
TSD=2.8 (data setup)
TSS=5.5 (select setup)
THD=1.7 (data hold)
THS=1.1 (select hold)
 (all times estimates)

ALL OUTPUTS EXIST AFTER CLOCK
clock= ^^ on C

MC160 12-bit Parity Generator/Checker

Sum of high inputs = Output

Even	Low
Odd	High

TPD=8.3 est

MC161 Binary 1 Of 8 decoder - low true outputs

E'	E'	S1	S2	S4	Q0'	Q1'	Q2'	Q3'	Q4'	Q5'	Q6'	Q7'
L	L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	L	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H
L	L	L	L	L	H	H	H	L	H	H	H	H
L	L	H	L	H	H	H	H	H	L	H	H	H
L	L	L	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	H	H	H	H	H	H	L	H
H	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	H	H	H	H	H	H	H	H

TPD=6.6 est

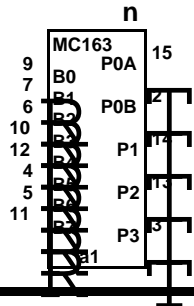
MC162 Binary 1 Of 8 decoder - high true outputs

E'	E'	S1	S2	S4	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	H	L	L	L	H	L	L	L	L	L	L
L	L	L	H	L	L	L	H	L	L	L	L	L
L	L	L	L	H	L	L	L	H	L	L	L	L
L	L	L	L	L	H	L	L	L	H	L	L	L
L	L	H	L	H	L	L	L	L	L	H	L	L
L	L	L	H	H	L	L	L	L	L	L	H	L
L	L	H	H	H	L	L	L	L	L	L	L	H
H	X	X	X	X	L	L	L	L	L	L	L	L
X	H	X	X	X	L	L	L	L	L	L	L	L

TPD=6.4

MC163

Error Detection/Correction Circuit



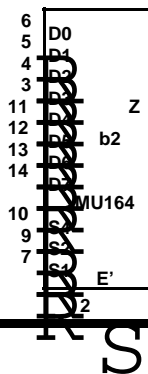
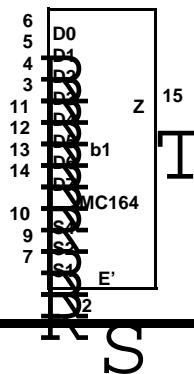
P0A = B1, B2, B4, B7
 P0B = B0, B3, B5, B6
 P1 = B1, B3, B5, B7
 P2 = B2, B3, B6, B7
 P3 = B4, B5, B6, B7

(, denotes EXOR)

Tpd=7.5 est

MC164

MU164



@(8)

8 line Multiplexer

E'	S1	S2	S4	Z
L	L	L	L	D0
L	H	L	L	D1
L	L	H	L	D2
L	H	H	L	D3
L	L	L	H	D4
L	H	L	H	D5
L	L	H	H	D6
L	H	H	H	D7
H	X	X	X	L

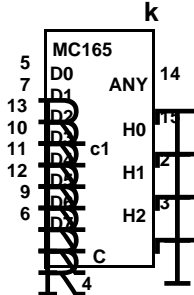
Midas multiplexer ONLY

Tpdd=4.8 (data)
 TpdS=6.5 (select)
 Tpde=3.1 (enable)

(all estimates)

MC165

8 input Priority Encoder with latch



D0	D1	D2	D3	D4	D5	D6	D7	ANY	H0	H1	H2
H	X	X	X	X	X	X	X	H	L	L	L
L	H	X	X	X	X	X	X	H	L	L	H
L	L	H	X	X	X	X	X	H	L	H	L
L	L	L	H	X	X	X	X	H	L	H	H
L	L	L	L	H	X	X	X	H	H	L	L
L	L	L	L	L	H	X	X	H	H	L	H
L	L	L	L	L	L	H	X	H	H	H	L
L	L	L	L	L	L	L	H	H	H	H	H
L	L	L	L	L	L	L	L	H	L	L	L

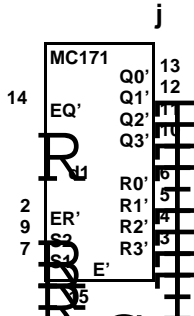
Tpdd=16.5 (data)
 TpdC= 5.3 (clock)
 Ts =5.1
 Th =0.0

(all estimates)

Outputs held when C is high

MC171

Dual Binary to 1-of-4 Decoder - low true outputs

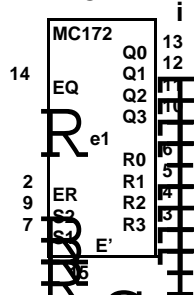


E'	EQ'	ER'	S1	S2	Q0'	Q1'	Q2'	Q3'	R0'	R1'	R2'	R3'
L	L	L	L	L	L	H	H	H	L	H	H	H
L	L	L	H	L	H	L	H	H	H	L	H	H
L	L	L	L	H	H	H	L	H	H	H	L	H
L	L	L	H	H	H	H	H	L	H	H	H	L
L	L	H	L	L	L	H	H	H	H	H	H	H
L	H	L	L	L	H	H	H	H	L	H	H	H
H	X	X	X	X	H	H	H	H	H	H	H	H

Tpd=6.4

MC172

Dual Binary to 1-of-4 Decoder - high true outputs

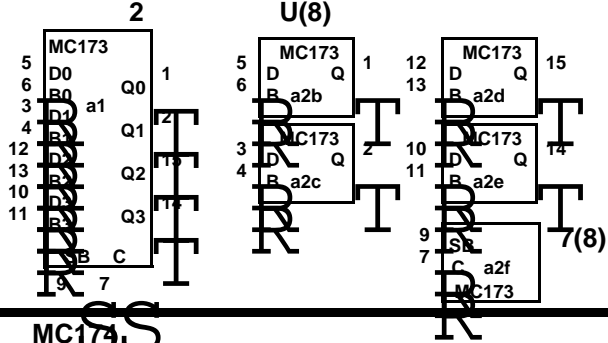


E'	EQ	ER	S1	S2	Q0	Q1	Q2	Q3	R0	R1	R2	R3
L	H	H	L	L	H	L	L	L	H	L	L	L
L	H	H	H	L	L	H	L	L	L	L	H	L
L	H	H	L	H	L	L	H	L	L	L	H	L
L	H	H	H	H	L	L	L	H	L	L	L	H
L	L	H	L	L	L	L	L	L	H	L	L	L
L	H	L	L	L	H	L	L	L	L	L	L	L
H	X	X	X	X	L	L	L	L	L	L	L	L

Tpd=6.4

MC173

Quad 2-input Multiplexer/Latch



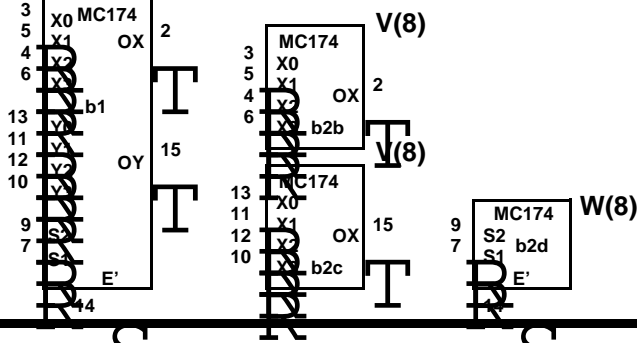
SB	C	Qi(n+1)
H	L	Bi(n)
L	L	Di(n)
X	H	Qi(n)

obsolete:

TP_{dd} = 5.3 (data)
TP_{dc} = 6.8 (clock)
TP_{ds} = 6.7 (select)
Th_d = 2.8 (hold data)
Th_s = 1.7 (hold select)

MC174

Dual 4 to 1 Multiplexer



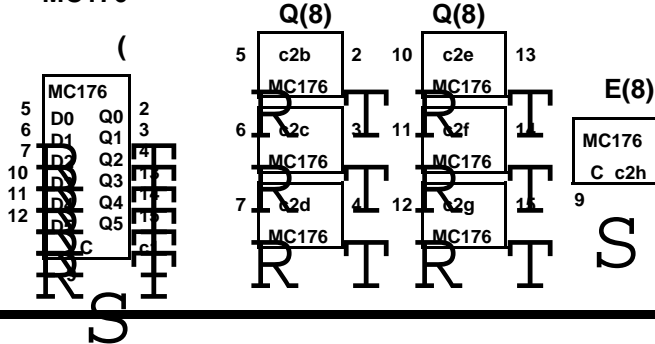
E'	S1	S2	OX	OY
H	X	X	L	L
L	L	L	X0	Y0
L	H	L	X1	Y1
L	L	H	X2	Y2
L	H	H	X3	Y3

obsolete:

TP_{dd} = 4.8 (data)
TP_{de} = 3.2 (enable)
TP_{ds} = 6.4 (select)

MC176

Hex D Master-Slave Flip-Flop



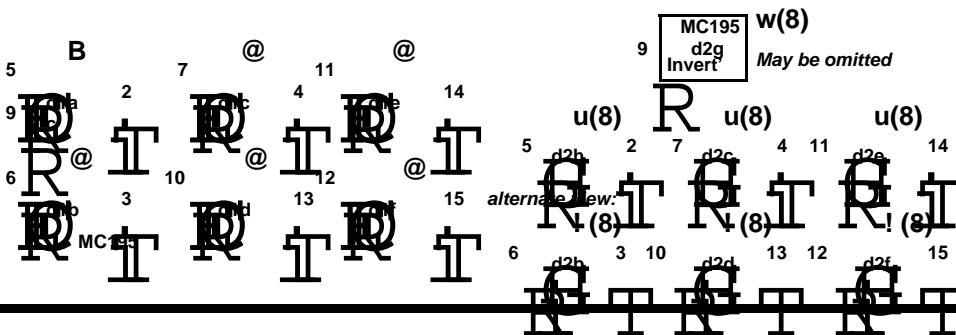
C	D	Qi(n+1)
L	X	Qi(n)
^^	L	L
^^	H	H

obsolete:

TP_d = 5.0
T_s = 2.8
Th = 1.7

MC195

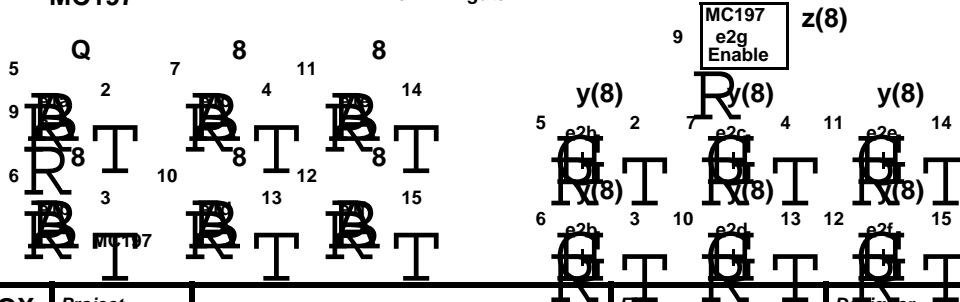
Hex Inverter/Buffer



TP_d = 4.2 **est**

MC197

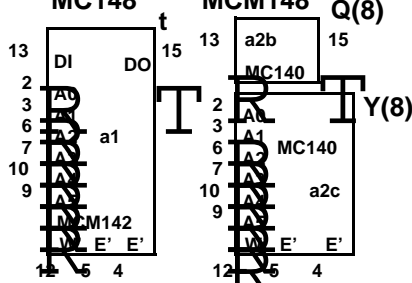
Hex AND gate



TP_{dd} = 4.2 (data) **est**
TP_{de} = 5.3 (enable) **est**

MC140 MCM140
 MC142 MCM142
 MC148 MCM148

64 Bit Random Access Memory



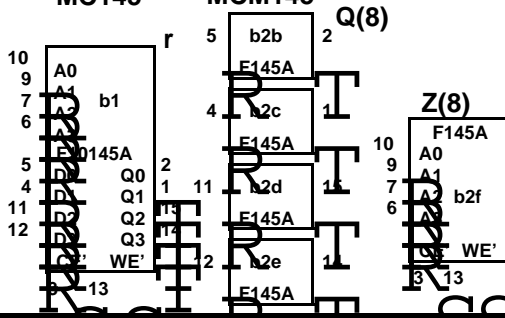
Tace=14 (E' access)
 Taad=11 (Ai access, MCM142)
 Taad=17 (Ai access, MCM140,148)
 Tw' =11 (write pulse width)
 Te' =15 (enable pulse width)
 (MCM140 drives 90 ohm loads)

Tsd=0 (setup times)
 Tse=3.5
 Tsa=5.5
 Thd=3.5 (hold times)
 The =0
 Tha=3.5
 (all times estimates)

F145A MCM145
 F10145A MCM145

16 x 4 Register File

obsolete: a(8) 5 b(8)



F10145:
 Tace=6.6 (E' access)
 Taad=9.9 (Ai access)
 Tw' =4.4 (write pulse width)
 Te' =4.4 (enable pulse width)
 Twr.=6.6 (ce,we output recover)
 MCM145:
 Tace=10 (E' access)
 Taad=15 (Ai access)
 Tw' =11 (write pulse width)
 Te' =11 (enable pulse width)

Tsd =5.0
 Tse =5.0
 Tsa =3.9
 Thd =1.0
 The =0.5
 Tha =1.0

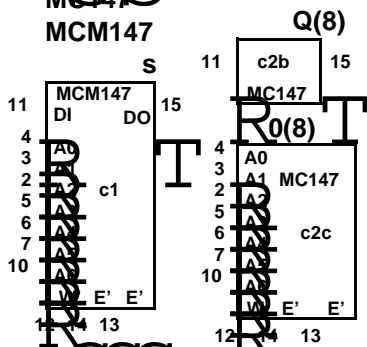
Tsd, Tse relative to end of WE'

Tsd =0 Thd =5.0
 Tse =5.0 The =5.0
 Tsa =5.0 Tha =5.0

all est

MC147 MCM147

128 x 1 bit Random Access Memory



Tace=8.8 (E' access)
 Taad=14 (Ai access)
 Tw' =8.8 (write pulse width)
 Te' =11 (enable pulse width)

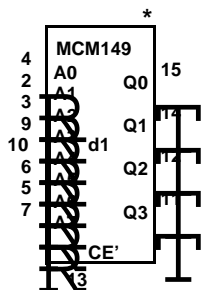
Tsd =1.0 (setup times)
 Tse =1.0
 Tsa =4.0

ALL UNUSED INPUTS MUST BE TIED TO VEE

Thd =1.0 (hold times)
 The =1.0
 Tha =3.0 (all times estimates)

MC149 MCM149
 MC150 MCM150

256 x 4 bit Programmable ROM



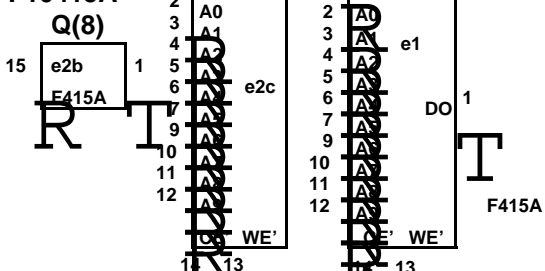
MCM149
 Tace=13
 Taad=32

MCM150
 Tace=10.5
 Taad=30

(all times estimates)

F415A F10415A

1024 x 1 bit Random Access Memory



Tace=10 (E' access)
 Taad=35 (Ai access) *
 Tw' =25 (write pulse width)
 Te' =35 (enable pulse width)

Tsd =5 (setup times)
 Tse =5
 Tsa =8

(all times estimates)

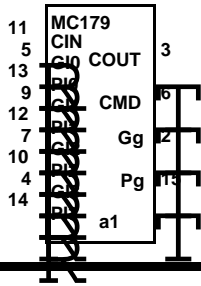
Thd =5 (hold times)
 The =5
 Tha =2

* a 25ns Taad, 20 ns. Tw' part is available

MC179

Look Ahead Carry Block

Tpd = 6 est



$$P_g = P_0 + P_1 + P_2 + P_3$$

$$G_g = (G_3 + P_2 + P_1 + P_0)(G_2 + P_1 + P_0)(G_1 + P_0)G_0$$

$$CMD = (CIN + P_3 + P_2)(G_3 + P_2)G_2$$

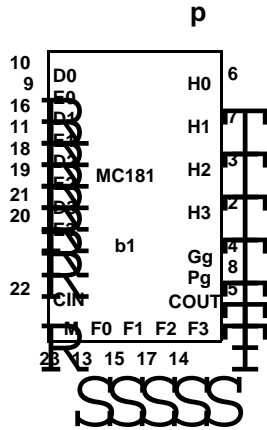
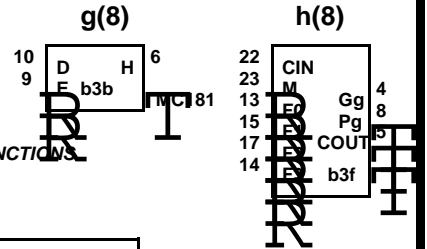
$$COUT = (CIN + P_0 + P_1 + P_2 + P_3)(G_3 + P_2 + P_1 + P_0)(G_2 + P_1 + P_0)(G_1 + P_0)G_0$$

MC181

4 bit ALU/Function Generator

LOGIC FUNCTIONS
M is HIGH

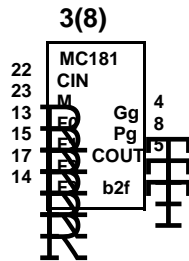
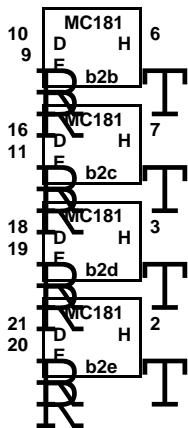
ARITHMETIC FUNCTIONS
M is LOW
CIN is LOW



F0	F1	F2	F3	H	H
L	L	L	L	D'	D PLUS 0
L	L	L	H	D' + E'	D PLUS (D AND E')
L	L	H	L	D' + E	D PLUS (D AND E)
L	L	H	H	all 1	D TIMES 2
L	H	L	L	D' AND E'	(D + E) PLUS 0
L	H	L	H	E'	(D + E) PLUS (D AND E')
L	H	H	L	D XNOR E	D PLUS E
L	H	H	H	D + E'	D PLUS (D + E)
H	L	L	L	D' AND E	(D + E') PLUS 0
H	L	L	H	D XOR E	D MINUS E MINUS 1
H	L	H	L	E	(D + E') PLUS (D AND E)
H	L	H	H	D + E	D PLUS (D + E')
H	H	L	L	all 0	MINUS 1 (2s complement)
H	H	L	H	D AND E'	(D AND E') MINUS 1
H	H	H	L	D AND E	(D AND E) MINUS 1
H	H	H	H	D	D MINUS 1

2(8)

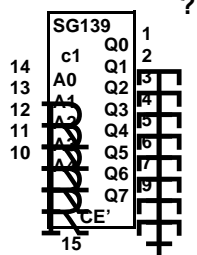
Tpd = 10.8 (max, all functions and carries)



SG10139

32 x 8 Programmable ROM

Tace=17.5
Taad=25 est



MC180 **I(8)** *Dual 1 bit Adder/Subtractor*

M0	M1	H
H	H	D PLUS E PLUS CARRY
H	L	D MINUS E MINUS CARRY
L	H	E MINUS D MINUS CARRY
L	L	0 MINUS D MINUS E MINUS CARRY

TPD=5.8 (all functions)

MC182 **2(8)** *2 bit ALU/Function Generator*

FO	F1	H	H
		M is HIGH	M is LOW
L	L	D XNOR E	D PLUS E PLUS CARRY
L	H	D XOR E	D' PLUS E PLUS CARRY
H	L	D AND E	D PLUS E' PLUS CARRY
H	H	D OR E	D TIMES 2

TPD=10.5 est

MC166 **q(8)** *5 bit magnitude comparator*

E'	X	Y	X<Y	X>Y
H	x	x	L	L
L	X=Y		L	L
L	X>Y		L	H
L	X<Y		H	L

TPDD=9.0 est
TPDE=3.8 est

MC158 **B(8)** **MC159** **C(8)** *Quad 2-to-1 multiplexers*

E'	Di	Bi	SB	Qi	Qi'
H	x	x	x		L
L	L	X	L	L	H
L	H	X	L	H	L
L	X	L	H	L	H
L	X	H	H	H	L

MC158 **TPDD=3.6** **MC159** **TPDD=3.6**
TPDS=5.0 **TPDS=5.0** **TPDE=5.0**
all times est

MC170 **D(8)** *9 bit parity circuit with 2 carry inputs*

SUM OF PINS 3-12	PIN 2	PIN 15
EVEN	L	?
ODD	H	?
SUM OF ALL INPUTS		
EVEN	?	L
ODD	?	H

TPDA=6.6 **TPDB=9.9** **TPDCARRY=3.3**
all times est