XEROX
PALO ALTO RESEARCH CENTER
Computer Science Laboratory
July 17, 1979

To: Route Users

From: Roger Bates

Subject: Timing analysis of nets

Stored: MAXC<Sil>NetDelays.press

The program called "NetDelays.run", found on MAXC<Sil>, is intended for helping the logic designer by providing some measure of the wire delay performance.

The program is invoked by: NetDelays/VDM Foo.wl

The file must be a wire-list file produced by the Route program. The results will be written onto a file called Foo.nd ("nd" for Net Delays).

> Output information is displayed on the screen as the wire list is processed. The program can be stopped by typing any character. You may then continue by typing any character, or skip the remaining nets by typing DEL.
>
> The optional switch V requests Verbose output, which will cause additional information to be displayed that may be of value in determining the nets performance. Program output will be described in gory detail below.
>
> The optional switch D disables output to the display and sends results only to the disk file.
>
> The optional switch M causes wire lengths to be computed as Manhatten (deltaX + deltaY), as opposed to the default straight line distance.

The output of this program contains Bravo format information specifying page headers, Tab stops, and Font 1. Bravo hardcopy will produce 2 columns per page of output (unless the Verbose switch was used). The output file is only reasonably formatted when read into Bravo and examined or printed by Bravo. It assumes that a small font (I have Helvetica8) is installed as font 1 in your User.cm for Bravo, and columns won't look good with larger fonts.

This program was written as a result of the Dorado project which uses ECL logic, and therefore the program is biased towards ECL. It ignores "Muffler" chips (a scheme of internal state sampling) as inputs, while including their pins for capacitive loading. It also recognizes "Selected ECL" chips as indicating nets involving clock distribution.

The next page contains an example of NetDelays output when run in the Verbose mode. The output that is only printed by Verbose mode is indicated by the use of italics.

> Additional summary information of net lengths and delays is printed on the last page of output. This information is self-explanatory and not shown here.

Muffler at a6
Clock at a8
Clock at a9
Muffler at b6
Found 4 Terminators

	CALIBRATE - skipped		
tiiiiiio	*15.1,8=4.3r*	alu.00(614)	Dly=4.3; L=7; T=1
itiiiiiiiiio	*15.4,13=5.3r*	5d BSel.2a(23)	Dly=5.3; L=11; T=1
tiiimiooit	*2.5,2=0.8w; 6.5,3=1.7f; 12.1,7=3.5r*	alub.00(233)	Dly=4.3; L=6; T=2; WO=1.6
otmioiit	*5.6,5=1.9w; 9,7=3f; 1.7,2=0.7r*	3w alua.00(223)	Dly=4.9; L=4; T=2; WO=3.8
omt		FF.0mem - skipped	
tmiiiiio	*10.5,6=3r*	LastNext.0'(229)	Dly=3.0; L=6; T=1
		GND132 - skipped	

The explanation of the output is as follows:

First a table is made indicating what locations contain "Mufflers" (ie MU10164) and "Selected Ecl" IC's. Then the nets are examined one at a time and reported as follows:

Each line starts with a string of characters that summarize the types of nodes on the net. The possible characters of "i o t m e" for input, output, terminator, muffler, and edge-pin respectively.

Edge pins will be treated as an "input" unless the net contains no output, then the edge pin will be assumed to be the "output".

After the net has been read in, three possible delay values are computed, and reported. The first is the delay between outputs(labeled "w"), the second is the delay from the first output to the last input(labeled "f"), and third is the delay from the first input to the last output(labeled "r").

The format of the report of this calculation is "d.d,p=t.t", where d.d is the distance between nodes (in inches), p is the number of pins between the nodes plus the end nodes, and t.t is the time for propagation (in nanoseconds).

Next the name of the net, and its "net number" as assigned by route, are printed. Notice that some net names are preceded by a 2(3) character "flag". The program examines the delay values for the nets, and "flags" those it thinks might be worth examining. The flag is made up of the delay in nanoseconds and a character indicating what check prompted the flag.

The possible flags are

- "5d " delay on a simple net
- "3w " delay between wire-or'd ouputs
- "3dc" delay on a net with a clock output
- "1wc" delay between outputs with a clock output

The numbers in these examples indicate the minimum delay that will prompt the flag.

"Dly=" the propagation time from the first input of the net, to the last output and back to the first output. This value is computed for both directions down the net, and the maximum is reported.

"L=" the total number of loads on the net, inputs including mufflers, but not terminators.

"T=" the number of terminators.

"WO=" the round-trip propagation delay between the outputs.

Now some comments about each of the nets in the above example:

CALIBRATE is skipped for obvious reasons.
alu.00 is an example of a simple net with only one output.
BSel.2a is a simple net, but has been flagged due to excessive net delay
alub.00 in an example of a multiple output net with good wire-or characteristics.
alua.00 is an example of a multiple output net flagged due to poor wire-or characteristics.
FF.0mem is skipped because its only input is a muffler, and that isn't interesting.
LastNext.0' is an example of a net where the muffler input is on the end of the net.

In this circumstance, the net delay calculated is from the first non-mufffler input on the left to the output on the right.

GND132 is skipped since it is a power net, as is VBB and VEE.

Multiple Boards

In order to allow net delays to be calculated on backpannel nets between boards, an additional slew of commands have been added to enable running NetDelays on multible wire list files.

NetDelays/W Foo.wl

The global switch "W" can be invoked on a single wire list file to cause NetDElays to select just the nets that touch edge pins (either E or C pins) and place them on a new file with the "wl" extension replaced with "Ewl". Using this on each board in a system will cause a series of ".Ewl" files to be created, which will later be used as the input wire list files to NetDelays for final backpannel processing. The advantages of this processs are 1) The Ewl files are relatively small so you should not run out of disk space 2) if minor edits are necessary (for signal name changes) are needed, Bravo can be used and finally 3) the NetDelays program will run faster.

NetDelays/EC FooTerms/T Foo1.ewl Foo2.ewl Blank Blank Foo3.Ewl

The global switch E or C are indications that NetDelays should process the edgepin nets for E pins or C pins respectively. I this case, the program expects a series of wirelist files, either complete ".wl" files, or the preselected ".Ewl" files, or a mixture of both.

The length of interconnections between boards is determined from the board dimensions found within the wirelist file togeather with the count of wirelist files between entries. Currently the program uses 0.7 inches between boards. As a means of declairing an unused socket within a series of .wl files, the reserved name Blank may be used in place of a board name. In the above example, there is .7 inches between Foo1 and F002, and ther is assumed to be 2.1 inches between boards Foo2 and Foo3.

For the problem of terminations, it is possible that terminating resistors might be implemented as part of the backpannel. If NetDelays is to be able to calculate the reasonableness of terminators, it must be told in some way about them. In the above example, the "FooTerms" is a text file which indicates 4 terminators associated with the socket for Foo1, 1 terminator for Foo2 and 5 terminators associated with the socket for Foo3. The contents of file FooTerms looks like:

Board 0
E0
E18
C1
C17

Board 1
E001

Board 4
E95
E96
C23
C24
C27

Running NetDelays on the above example might produce the following output on file F001.End

0=;File=Foo1.sil Rev=Ba Date=11/2/78 Page=01 -MARKED BUILT-
1=;File=Foo2.sil Rev=Ba Date=11/2/78 Page=01 -MARKED BUILT-
2=;Blank
3=;Blank
4=;File=Foo2.sil Rev=Ba Date=11/2/78 Page=01 -MARKED BUILT-

tiiiiioooie0,toe1,> 21.9,10=5.8r	*5d FG.0(22.7)*	*Dly=5.8; S=4; L=6; T=2*
iiiiioooiet1,etot4,> 12.1,10=4.1r	*3T FG.1(21.1)*	*Dly=4.1; S=4; L=6; T=3; Stub=4.6*
tiie0,tie4,> 22.1,3=4r	*0S Signal2(22.1)*	*Dly=4.0; S=0; L=3; T=2*
tiie0,> 22.1,3=4r	*1B Signal1(22.1)*	*Dly=4.0; S=0; L=2; T=1*

Unused backpannel terminator on Board 4 Pin E96.

Total Nets = 5
Average Net Length = 22.000 (based on Euclidean wire routing)
Average Net Delay = 4.320

Total Nets with delays between 3 and 4 ns = 1
Total Nets with delays between 4 and 5 ns = 3
Total Nets with delays between 5 and 6 ns = 1

In Verbose mode, the net is characterised by the node strings ("tiioe") followed by the board number that the net is from, and separated by commas.

The reasons and minimum values for "flagging" a net are different in the EdgePin mode.

The possible flags are

"1B "	The net only goes to one board
"3T "	The net contains to many terminators
"0L "	The net contains no inputs (Loads)
"0S "	The net contains no outputs (Sorces)
"1sc"	The clock net contains a "stub" which could cause a pulse of width >1
"3s "	The net contains a "stub" which could cause a pulse of width >3
"3dc"	The clock net has a delay >3
"5d "	The clock net has a delay >5