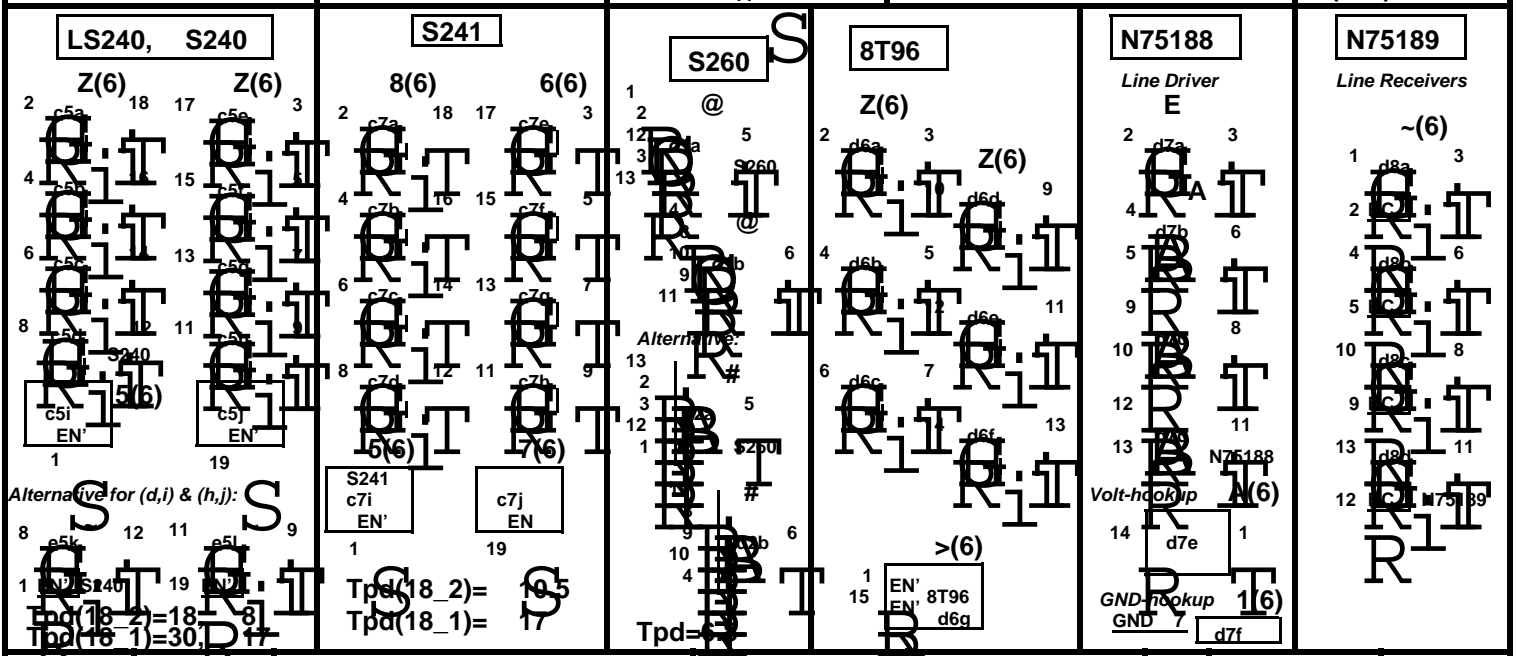
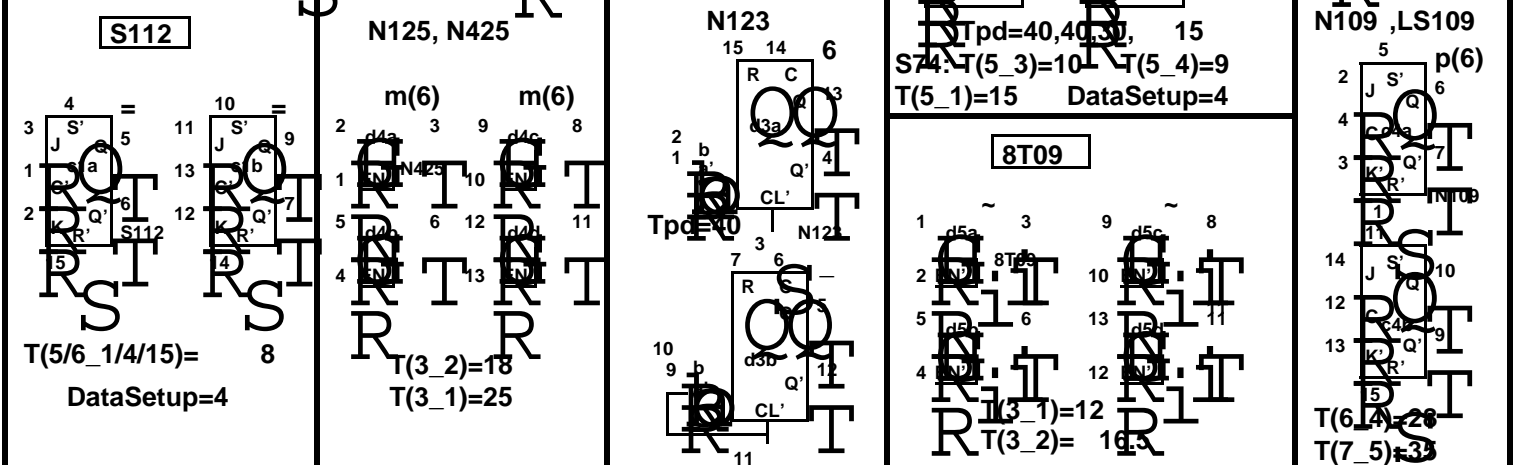
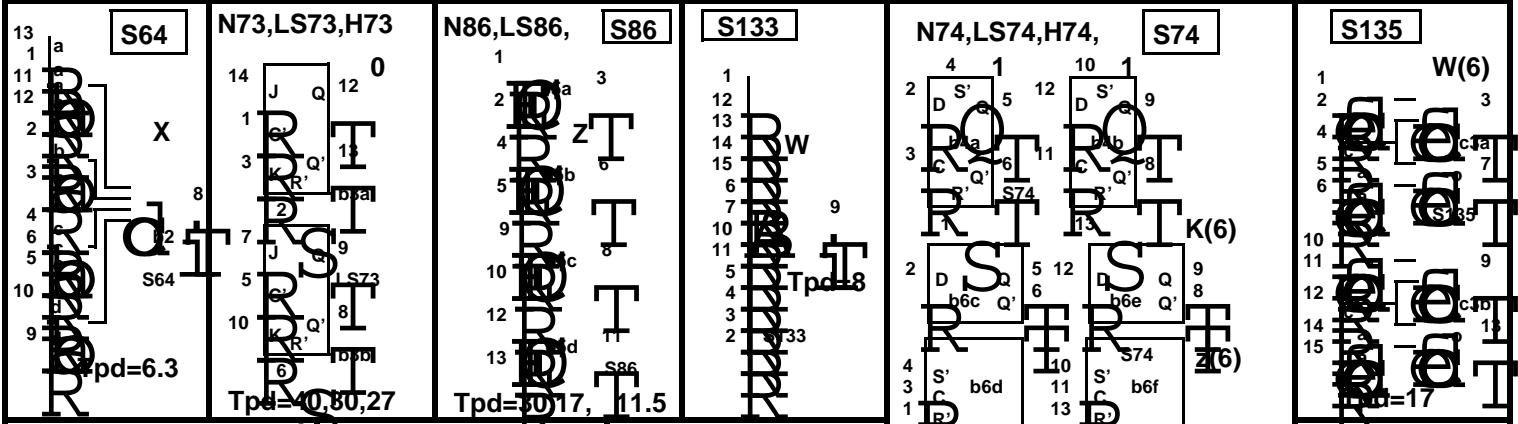
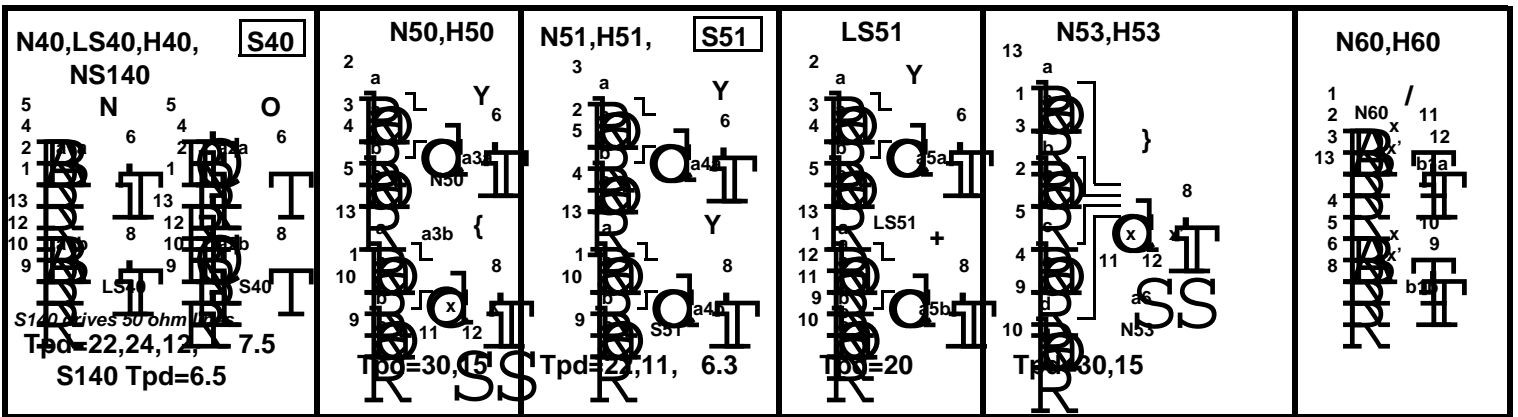
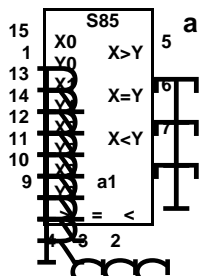


<p>N00,LS00,H00, S00</p>	<p>N01,LS01</p>	<p>N02,LS02, S02</p>	<p>N03,LS03,S03</p>	<p>N04,LS04,H04, S04</p>
<p>N05,LS05,H05,S05</p>	<p>N06</p>	<p>N07</p>	<p>N08,LS08, S08</p>	<p>N09,LS09</p>
<p>N10,LS10,H10, S10</p>	<p>N11,LS11,H11, S11</p>	<p>N20,LS20,H20, S20</p>	<p>N25</p>	<p>N27,LS27</p>
<p>N28,LS28, N128</p>	<p>N30,LS30,H30, S30</p>	<p>N32,LS32, S32</p>	<p>N37,LS37, S37</p>	<p>N38,LS38, S38</p>



N85, S85

4 Bits Comparator



X	Y	>	=	<	X>Y	X=Y	X<Y
X>Y	X	X	X	H	L	L	L
X<Y	X	X	X	L	L	H	H
X=Y	L	L	H	L	L	H	H
X=Y	L	H	L	L	H	L	L
X=Y	H	L	L	H	L	L	L

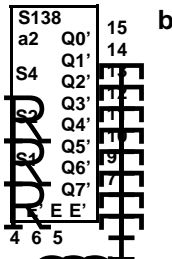
For other states, see catalog

X0/Y0 is the MostSignificant bit
X3/Y3 is the LeastSignificant bit

	Tpd	N85	S85
X,Y X>Y		30	18
X,Y X<Y		30	18
X,Y X=Y		35	20
< X>Y	17		9.5
= X>Y	17		9.5
= X=Y	20		12
< X<Y	17		9.5
= X<Y	17		9.5

LS138, S138

Binary 1 of 8 Decoder



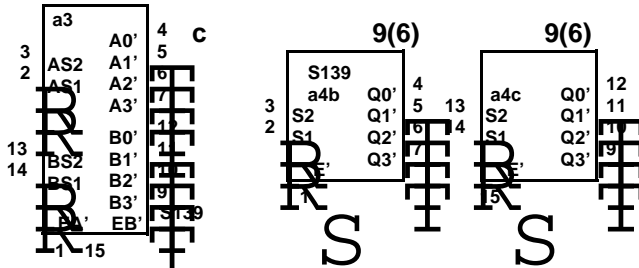
E'	E	E'	S4	S2	S1	Q0'	Q1'	Q2'	Q3'	Q4'	Q5'	Q6'	Q7'
L	H	L	L	L	L	L	H	H	H	H	H	H	H
L	H	L	L	L	H	L	H	H	H	H	H	H	H
L	H	L	L	H	L	H	H	L	H	H	H	H	H
L	H	L	L	H	H	L	H	H	L	H	H	H	H
L	H	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	L	H	H	H	H	H	H	L	H	H
L	H	L	H	H	L	H	H	H	H	H	H	L	H
L	H	L	H	H	H	H	H	H	H	H	H	H	L
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H

	Tpd	LS138	S138
S to Out		41	13.2
Enable		38	12

Q0' is the MostSignificant bit
Q7' is the LeastSignificant bit

LS139, S139

Dual Binary 1 of 4 decoder



S2	S1	E'	0'	1'	2'	3'
X	X	H	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
H	L	L	H	H	L	H
H	H	L	H	H	H	L

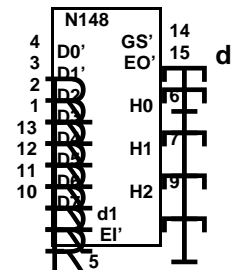
Each Section

A0'/B0' is the MostSignificant bit
A3'/B3' is the LeastSignificant bit

	Tpd	LS139	S139
S to Out		38	13.2
Enable		32	11

N148

8 Line Priority Encoder



EI' = Enable In (cascade)
EO' = Enable Out
GS = Group Select (EOvEI')
D0' is highest priority with 000 on outputs when asserted

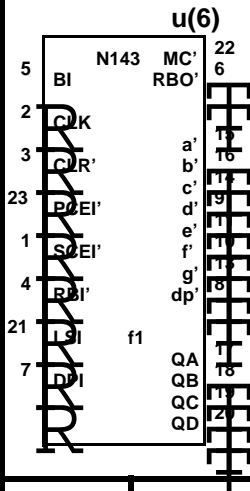
D0' is the MostSignificant bit
D7' is the LeastSignificant bit

H0 is the MostSignificant bit
H2 is the LeastSignificant bit

Tpd D to H =	21
Tpd D to EO =	27.5
Tpd D to GS =	33
Tpd EI to H/GS =	17
Tpd EI to EO =	33

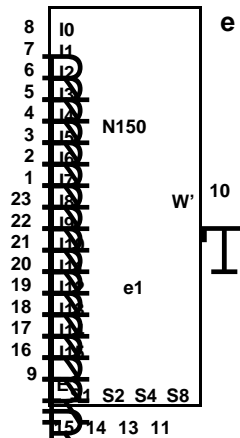
N143

4-bits Count/Latch/LED Drivers



N150

1 of 16 multiplexor



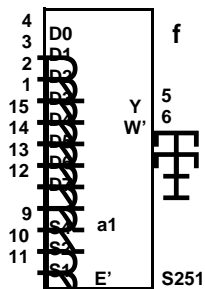
S8,S4,S2,S1=	0000	selects	I0
S8,S4,S2,S1=	0001	selects	I1
S8,S4,S2,S1=	0010	selects	I2
S8,S4,S2,S1=	0100	selects	I4
S8,S4,S2,S1=	1000	selects	I8
S8,S4,S2,S1=	1111	selects	I15

Tpd select to out 35
tpd input to out 20
Tpd Enable to out 30

I0 is the MostSignificant bit
I15 is the LeastSignificant bit

N151,LS151, S151 N251,LS251, **S251**

1 of 8 Multiplexor



S4,S2,S1=000 selects D0
 S4,S2,S1=001 selects D1
 S4,S2,S1=010 selects D2
 S4,S2,S1=100 selects D4
 S4,S2,S1=111 selects D7

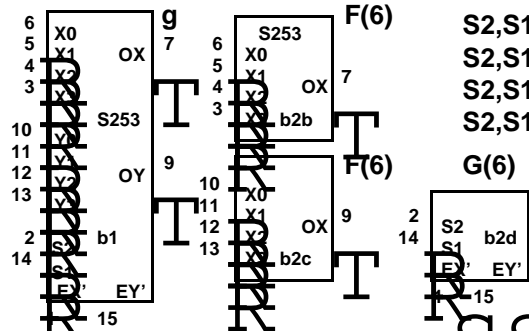
	151	251
Tpd S to Y=38,50,	20	45,45, 21.5
Tpd S to W'=30,39,	16.5	33,33, 17
Tpd D to Y=27,32,	13.5	28,28, 13.5
Tpd D to W'=14,21,	8	15,15, 8
Tpd E to Y=33,42,	20	40,40, 23
Tpd E to W'=23,31,	14.5	40,40, 23

251 has Tri State Outputs

D0 is the MostSignificant bit, D7 is the LeastSignificant bit

N153,LS153, LS253(AM74LS253), S153, **S253(AM74S253)**

Dual 1 of 4 multiplexors

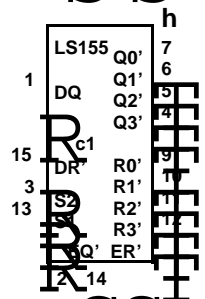


S2,S1=00 selects X0(Y0)
 S2,S1=01 selects X1(Y1)
 S2,S1=10 selects X2(Y2)
 S2,S1=11 selects X3(Y3)

Tpd S to O=34,38,30,	20,20
Tpd Data to O=23,26,15,	10,10.5
Tpd E to O=30,32,25,	16.5,23

X0/Y0 is the MostSignificant bit, X3/Y3 is the LeastSignificant bit

N155,LS155 **S155** Dual 2 to 4 decoders



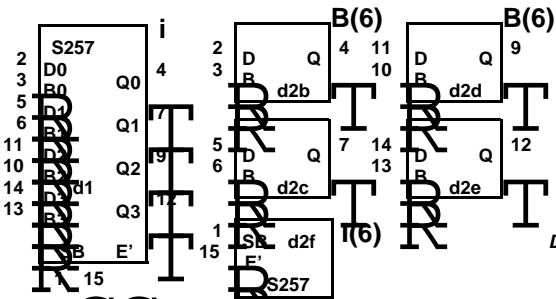
S2,S1=00 selects Q0'(R0')
 S2,S1=01 selects Q1'(R1')
 S2,S1=10 selects Q2'(R2')
 S2,S1=11 selects Q3'(R3')

Tpd S to Q(R)=32,30
Tpd DQ' to Q=30,27
Tpd DR to R=32,30
Tpd E to Q(R)=27,30

Q0'/R0' is the MostSignificant bit, Q3'/R3' is the LeastSignificant bit

N157,LS157, S157, **S257**

Quad 2 to 1 multiplexors (non inverting outputs)



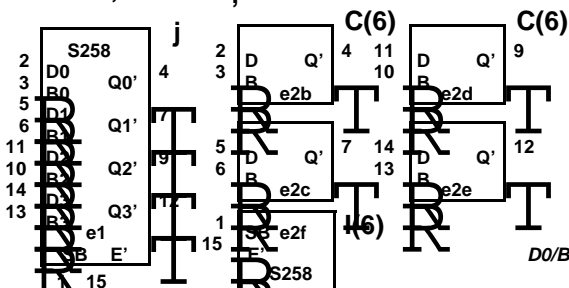
SB=0 selects D
 SB=1 selects B

Tpd SB to Q=27,27,	16.5,16.5
Tpd E' to Q=21,21,	14,23
Tpd D/B to Q=14,14,	8.5,8.5

D0/B0/Q0 is the MostSignificant bit, D3/B3/Q3 is the LeastSignificant bit

LS158, S158, **S258**

Quad 2 to 1 multiplexors (inverting outputs)

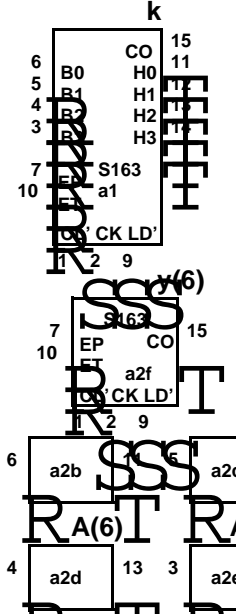


SB=0 selects D
 SB=1 selects B

Tpd SB to Q'=24,	13.2
Tpd E' to Q'=18,	13.2
Tpd D to Q'=12,	7

D0/B0/Q0' is the MostSignificant bit, D3/B3/Q3' is the LeastSignificant bit

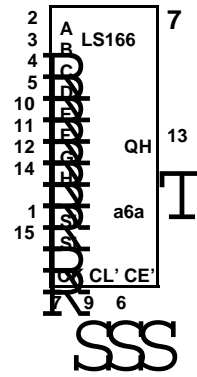
N160-N163,LS160-LS163, S162- S163 Four bit counters



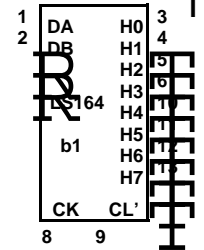
160/161 are decade counters
 160/162 has direct clear
 161/163 are binary counters
 162/163 has synchronous clear
 EP is parallel enable (doesn't affect CO)
 ET is ripple carry enable (affects CO)
 min clock pulse width=25,25, 11
 min clear pulse width=20,20, 11
 setup load=25,20, 16 hold load=0,0, 0
 setup EP=20,20, 14 hold EP=0,0, 5
 Tpd clock to Q=23,27, 17 (count)
 Tpd clock to Q=29,29, 17 (load)
 Tpd clock to CO=35,35, 28
 Tpd ET to CO=16,23, 17
 Tpd CL' to Q=38,28, ? (direct clear only)
 setup CL'=20,20, 16 hold CL'=0,0, 0
 setup data=20,20, 5 hold data=0,0, 4

B0/H0 is the MostSignificant bit
 B3/H3 is the LeastSignificant bit

LS166, N166 8 bits P/S shifter

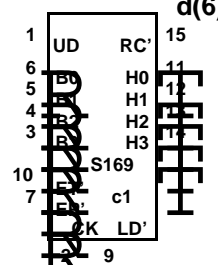


N164,LS164 8 bit parallel-out serial shift register



DA and DB must both be high for a 1 to get shifted in (they are Anded together)
 Asynchronous clear
 width of clock or clear min=20
 Tpd 37,32 hold=5,5
 tpd clear=42,36
 Data setup=15,15

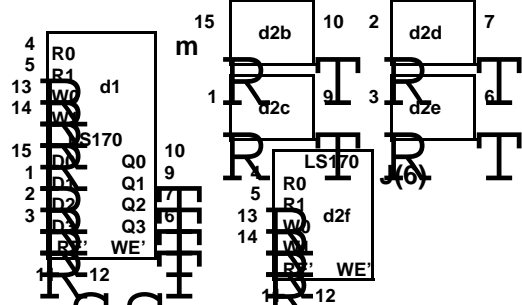
S169 LS169 4-bits Up/Down Binary Counters



Tpd CK to H's= 17
 Tpd CK to RC'= 30
 Tpd UD to RC'= 24
 Tpd ET' to RC'= 27
 min clock pulse= 12
 setup data= 5 setup load= 7
 setup EP'/ET'= 16 setup UD= 22

B0/H0 is the MostSignificant bit
 B3/H3 is the LeastSignificant bit

N170,LS170,LS670 A(6) 4 by 4 Register Files

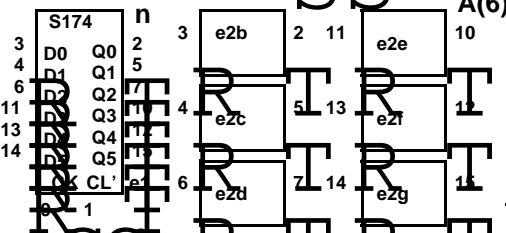


R0 and R1 select read address
 W0 and W1 select write address
 RE' is output enable
 WE' is write enable
 170s have OC outputs
 LS670 has tristate outputs

Tpd R0/R1 to Q=40,40,45
 Tpd RE to Q=30,30,35-50
 Tpd WE to Q=45,45,50
 Tpd D to Q=45,45,45
 Data setup=10 hold=15
 min width of write pulse=25

R0/W0 is the MostSignificant bit
 R1/W1 is the LeastSignificant bit

N174,LS174, S174 Hex D Registers



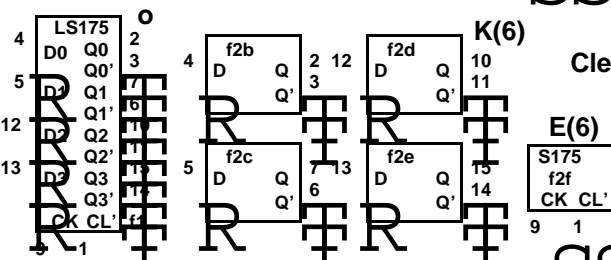
Clear is asynchronous

clock pulse width min=20,20, 9
 clear pulse width min=20,20, 14
 clear inactive to clock min=25,25,

Tpd CK to Q=30,30, 19
 Tpd CL' to Q=35,35, 25

Data setup=20,20, 6
 Data hold=5,5, 4

N175,LS175, S175 Quad D registers with Q and Q' outputs



Clear is asynchronous

clock pulse width min=20,20, 9
 clear pulse width min=20,20, 14

Tpd CK to Q=30,30, 19
 Tpd CL' to Q=35,35, 25

Data setup=20,20, 6
 Data hold=5,5, 4

N180 *9 bit ODD/EVEN parity generator/checker*

EVI and OVI are cascading inputs

Timing:
 Tpd IN to EVN=68 (OVI grounded)
 Tpd IN to EVN=48 (EVI grounded)
 Tpd IN to ODD=48 (OVI gnded)
 Tpd IN to ODD=68 (EVI gnded)
 EVI/OVI to EVN/ODD=20

N181, LS181, S181 *Arithmetic Logic Unit*

Timing:
 Tpd CIN to COUT=19,27, 12
 Tpd D/E to COUT(Sum)=43,38, 21
 Tpd D/E to COUT(Diff)=50,41, 26.5
 Tpd CIN to H=19,26, 14
 Tpd D/E to Pg/Gg(Sum)=19,30, 14
 Tpd D/E to Pg/Gg(Diff)=25,33, 17
 Tpd D/E to H (Sum)=42,32, 19
 Tpd D/E to H (Diff)=48,32, 25
 Tpd D/E to H (Logic)=48,38, 25
 Tpd D/E to "A=B"=50,62, 35

*D0/E0/H0 is the MostSignificant bit
 D3/E3/H3 is the LeastSignificant bit
 F0 to F3 are function controls (S3 to S0 in TI Data Book)*

N182, S182 *Lookahead carry generator*

Timing:
 Tpd G/P to C=22, 8
 Tpd G/P to Pg=22, 11
 Tpd G/P to Gg=22, 11.5
 Tpd CIN to CZ=?, 11.5

*G10'/P10' is the MostSignificant bit
 G3'/P3' is the LeastSignificant bit
 CZ is the MostSignificant bit
 CX is the LeastSignificant bit*

N188, N288, S188, S288 *32 by 8 PROM*

**188 is OC outputs
 288 is Tri-state**

**Address Access=50,50,30,30
 Enable Access=50,50**

N190, N191, LS190, LS191 *Synchronous Up/Down Counters with Mode Control*

**190s are decade counters
 191s are binary counters
 UD=0 for up count, 1 for down count
 Change CE only when CK is high
 LD is asynchronous RC is ripple carry
 MM is max/min output (no carry in)
 Min width CK=25, min width LD=35
 Data setup=25, Data hold=0**

Timing:
 Tpd CK to H=36
 Tpd LD to Q=50
 Tpd B to H=50
 Tpd CK to MM = 52
 Tpd CK to RC=24
 Tpd UD to RC=45
 Tpd UD to MM=33

*B0/H0 is the MostSignificant bit
 B3/H3 is the LeastSignificant bit*

N192, N193, LS192, LS193 *Synchronous Up/Down Counters with Dual clock*

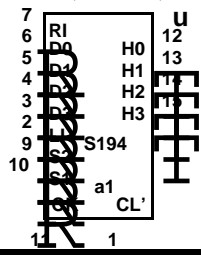
**192s are decade counters
 193s are binary counters
 Hold one clock input high when pulsing other clock
 LD is asynchronous Clear is asynchronous
 BO is fed forward from CD CO is fed forward from CU
 Min width CK,LD or CL=20, data setup=20, hold=0**

Timing:
 Tpd CK to H=47
 Tpd LD to H=40
 Tpd CL to H=35
 Tpd CU to CO=26
 Tpd CD to BO=24

*B0/H0 is the MostSignificant bit
 B3/H3 is the LeastSignificant bit*

N194,LS194, S194

4 bit Bidirectional shift register



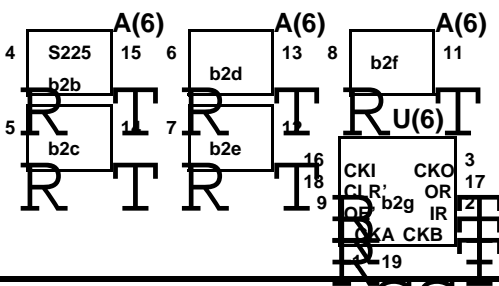
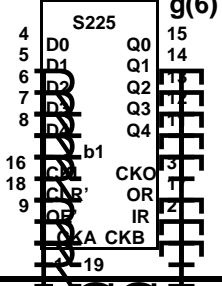
S2	S1	operation
H	H	load
L	H	shift right (H1 gets H0)
H	L	shift left (H0 gets H1)
L	L	Do nothing

Clear is asynchronous
D0/H0 is the MostSignificant bit
D3/H3 is the LeastSignificant bit

Tpd CK to H=26,47, 18.5
Tpd CL' to H=30,54, 20.5
Data setup=20,20, 6
Mode setup=30,30, 12
All holds=0,0, 4
min width Clock=20,20, 9
min width Clear=20,20, 14
min Clear Inactive=20,20, 10

S225

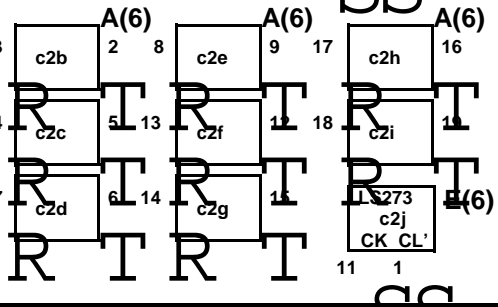
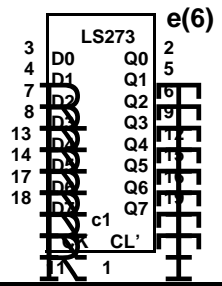
16 by 5 FIFO Memory



See catalog for timing

LS273

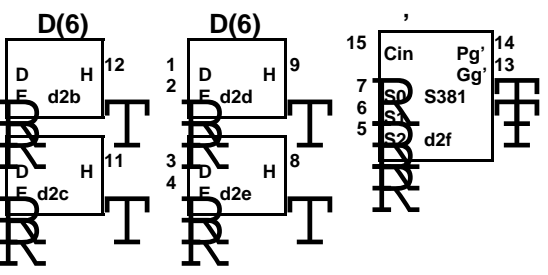
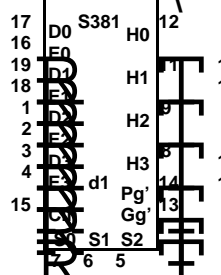
Octal D-Flip-Flop



Tpd CK to Q= 30
Tpd CL' to Q= 30

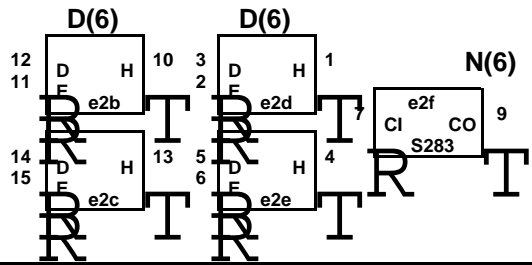
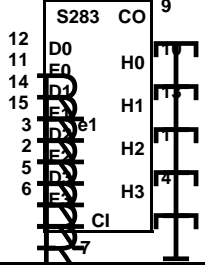
LS381, S381

4 bits Arithmetic Logic Unit



N283,LS283, S283

Four Bit adder

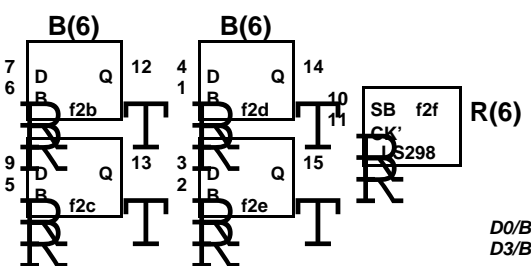
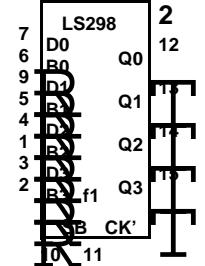


Tpd D/E to H=24,24, 20
Tpd CI to H=21,24, 20
Tpd CI to CO=16,17, 12.5
Tpd D/E to CO=16,17, 13.5

D0/E0/H0 is the MostSignificant bit
D3/E3/H3 is the LeastSignificant bit
CI is the Carry Input
CO is the Carry Output

N298,LS298

Quad 2 input multiplexor/register



SB=0 selects D inputs
SB=1 selects B inputs

Tpd CK' to Q = 32
Min width CK' = 20
Data Set-up=15
Data Hold=5
SB setup=25
SB Hold=0

Clock on negative transition

D0/B0/Q0 is the MostSignificant bit
D3/B3/Q3 is the LeastSignificant bit

S374 f(6) *Octal D-type Tri-state FlipFlop with Enable*

OC'	CK	D	Qn
L	^^	H	H
L	^^	L	L
L	L	X	Q _{old}
H	X	X	Off

For S373 use \ (6) instead of f(6) and use / (6) instead of T(6) at pin 11 is EN instead of CK

Tpd CK to Q= 19
Tpd OC' to Q= 20
min width clock= 9.5
setup data= 6
hold data= 3

S378 X(6) *67S378 by MMI Octal D-type Tri-state FlipFlop with Enable and Inverted Outputs*

OC'	CK	D	Qn'
L	^^	H	L
L	^^	L	H
L	L	X	Q _{old}
H	X	X	Off

Tpd CK to Q= 19
Tpd OC' to Q= 20
min width clock= 9.5
setup data= 6
hold data= 3

AM25S09 S(6) *Quad Two Input High Speed Register*

SB	CK	D	Q
0	0	0	0
0	0	1	1
0	1	X	Q _{old}
1	X	X	Off

Tpd CK to Q= 19
min clock width= 9
set data= 7 hold data= 4
set SB= 12 hold SB= 4
SB=0 for D inputs
not compatible with 298

AM25S10 a(6) *4 bits four-ways Shifter with Tristate Outputs*

Tpd I to Y=12
Tpd S to Y=20
Tpd OE to Y=21

AM25S18 9 *Quad Register with both totem pole and Tristate Outputs*

F9401 CRC Generator/Checker

S280 9 bit Even/Odd parity generator/checker

Tpd IN to EVN/OD = 23

MCT6 @ (6) *Dual Opto-Isolator (2 8 pins packages)*

Output is isolated from Input and Power supply

Made by Monsanto

F93422 h(6) *Fairchild 256 by 4 RAM*

CE'	WE'	OE'	Q
0	0	0	0
0	0	1	1
0	1	X	Q _{old}
1	X	X	Off

Tpd CE' to Q= 30
Tpd A to Q= 45
min write pulse= 30
setup address= 10
setup data= 5
setup CE= 5
hold address= 5
hold data= 5
hold CE= 5
write recovery= 40

i2147 1024 by 1 RAM

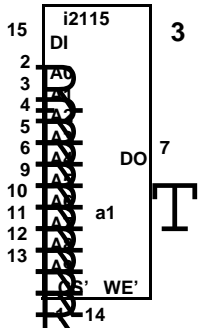
To replace AM9135J

i2115,i2125,F93415A,

F93425A

1K by 1 RAM

intel,fairchild



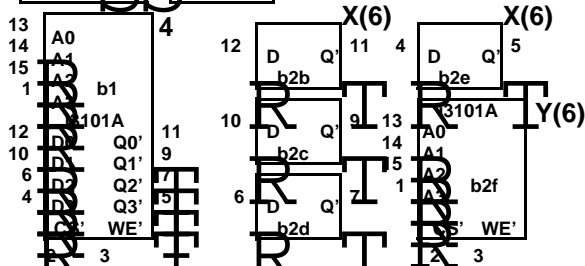
2115 and 93415 are OC output
 2125 and 93425 are tristate outputs

Address Access=70,45
 Chip Select=40,30
 Chip Select recovery=40,30
 Write pulse min=35,50
 Data Setup=5,5 Hold=5,5
 Address setup=15,5 Hold=5,5

See data sheets for more information on write cycles

i3101A, S189

16 by 4 RAM



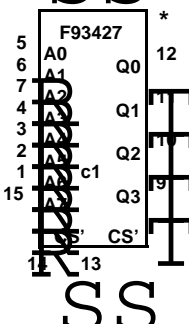
Address Access=35
 Chip Select=17
 Sense Amp Recovery=35
 Write pulse min=25
 Address setup/hold=0

Data stable prior to l to h transition on WRITE=25

i3601, 3621,

F93427

256 by 4 PROM

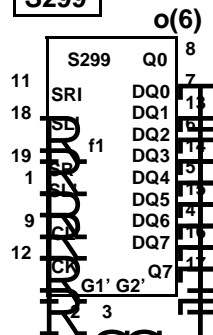


Address Access=50, 40
 Enable Access=25,25

A0 is the MostSignificant bit
 A7 is the LeastSignificant bit
 Q0 is the MostSignificant bit
 Q3 is the LeastSignificant bit

S299

8-bits Universal Shift/Storage Register



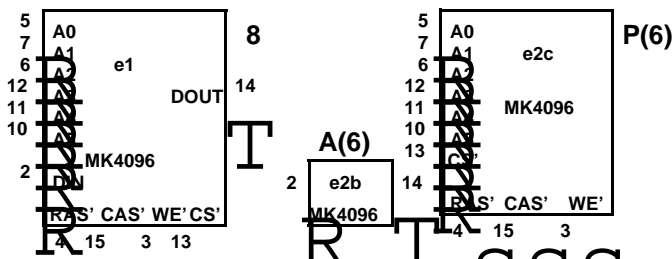
See TI Databook Page 7-437

Tpd CK to DQ = 23
 Tpd CL to DQ = 24
 Tpd G's to DQ = 20
 min width clock = 12
 setup data = 8
 hold data = 5

Q0 is the MostSignificant bit
 Q7 is the LeastSignificant bit

MK4096

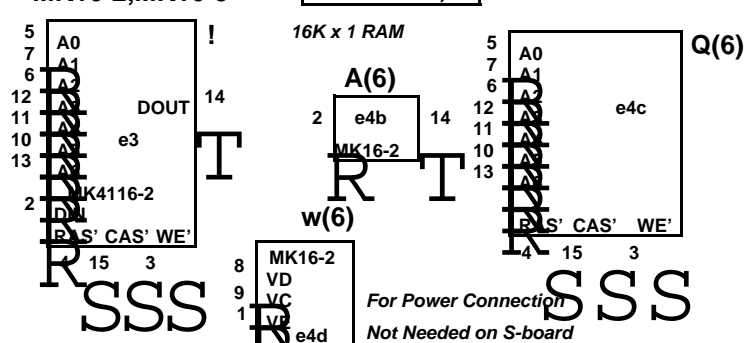
4K by 1 RAM



See Data Sheet for timing specs

MK16-2, MK16-3

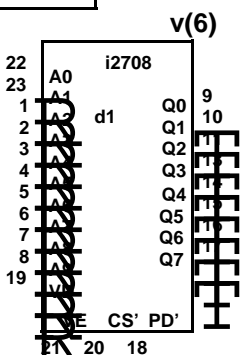
MK4116-2, MK4116-3



See Data Sheet for timing specs

i2708

1K by 8 EPROM



T(Q_A)=450

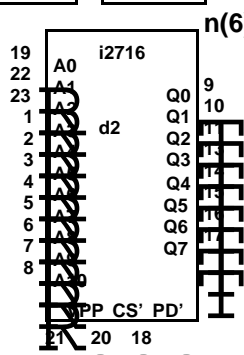
See Data Sheet

Note pin numbers are not
 all same as in catalogue

i2716

i2758

2Kx8 EPROM (2716), 1Kx8 EPROM (2758)



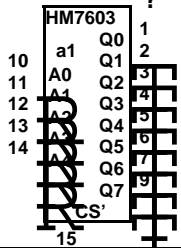
T(Q_A)=450

See Data Sheet

Note pin numbers are not
 all same as in catalogue

HM7603

Harris 32X8 PROM



A0 is the MostSignificant bit
A4 is the LeastSignificant bit

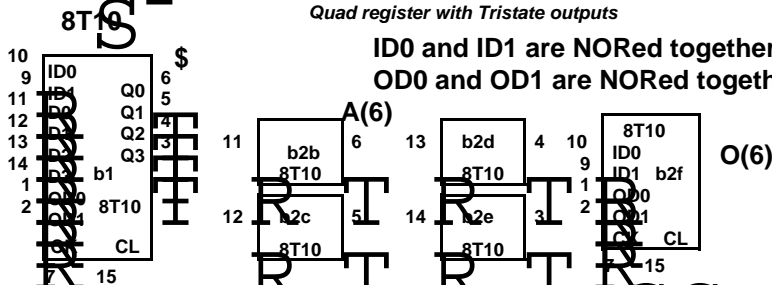
Q0 is the MostSignificant bit
Q7 is the LeastSignificant bit

TPD A's to Q=40
TPD CS' to Q=30

Quad register with Tristate outputs

ID0 and ID1 are NORed together
OD0 and OD1 are NORed together

TPD CK to Q= 28
TPD OD to Q= 33
TPD CL to Q= 24
Data setup= 6
Data hold= 6
min clock width= 14
min clear width= 17



D0/Q0 is the MostSignificant bit
D3/Q3 is the LeastSignificant bit

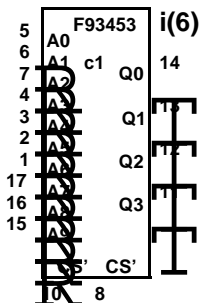
F93453

1K by 4 PROM

FPLAT

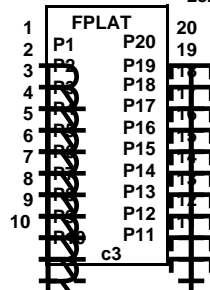
0(6)

20 pins PlatForm



TPD A's to Q= 50
TPD CS' to Q=30

A9 is the LeastSignificant bit
Q3 is the LeastSignificant bit



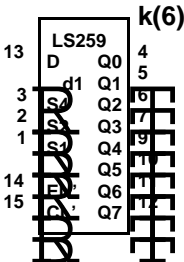
pin #10 is grounded
pin #20 is VCC (+5v)

LS259

8-bits Addressable Latches

S4	S2	S1	Latch
L	L	L	Q0
L	L	H	Q1
L	H	L	Q2
L	H	H	Q3
H	L	L	Q4
H	L	H	Q5
H	H	L	Q6
H	H	H	Q7

T(Q_CL')=27
T(Q_D)=32
T(Q_S's)=38
T(Q_EN')=35
T setup=15



CL'	EN'	Addressed OutPut	Other OutPut
L	L	D	L
L	H	L	L
H	L	D	Q _{old}
H	H	Q _{old}	Q _{old}

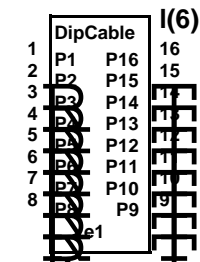
Q0 is the MostSignificant bit
Q7 is the LeastSignificant bit

DipCable

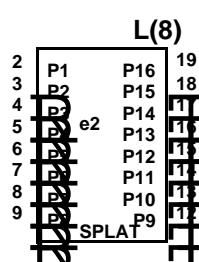
Dip for 16 lines Cable

SPLAT

16 pins PlatForm

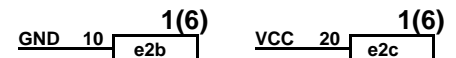


Note Pin#8 is grounded



Note it is staffed in the middle of a 20 pins position on S-board so to avoid GND and VCC

Added the following subgroups in your drawings if you do not want the trace-wire of GND & VCC to be CUT:

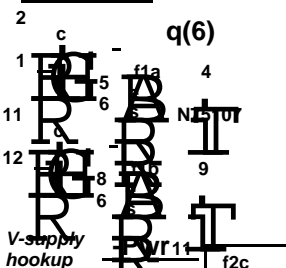


N75107

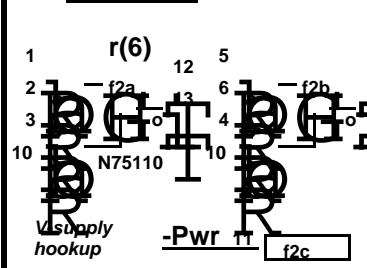
Dual Line Receivers

N75110

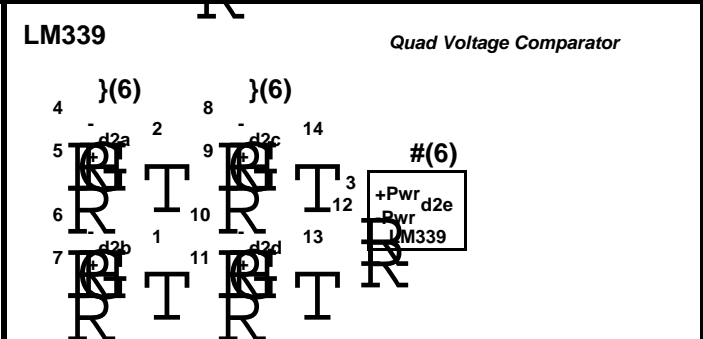
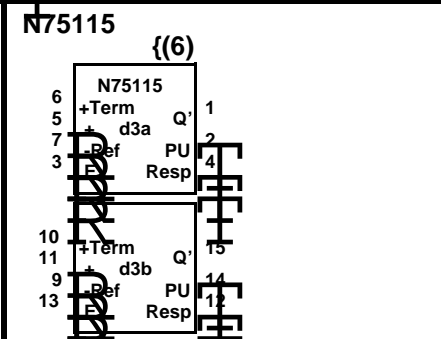
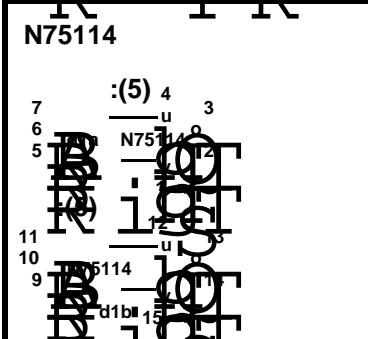
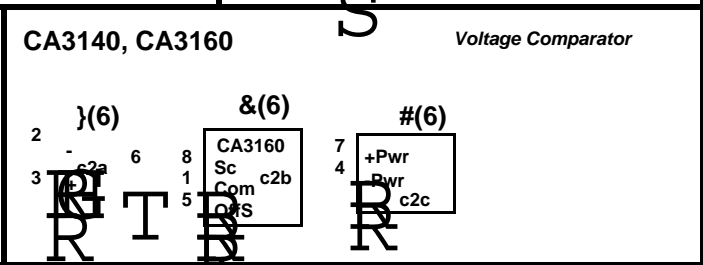
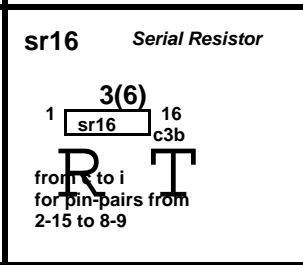
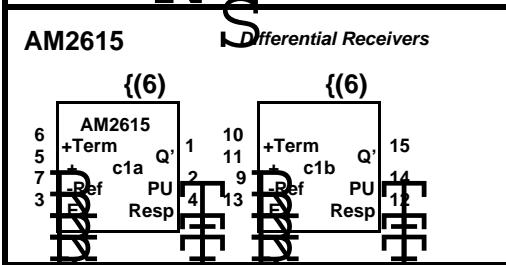
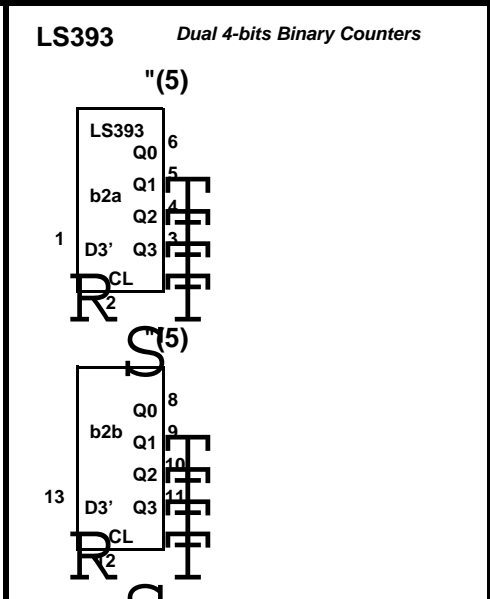
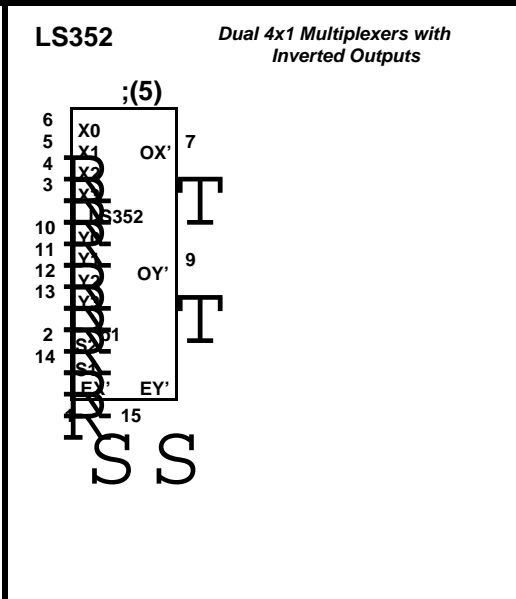
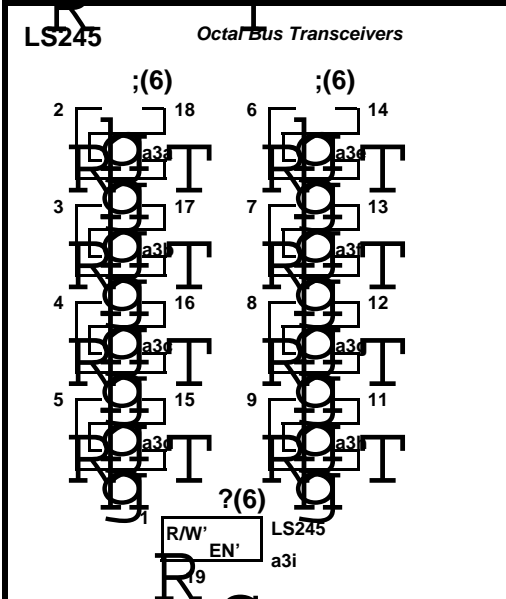
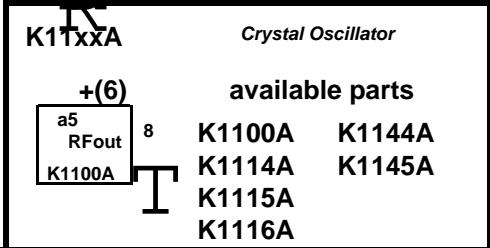
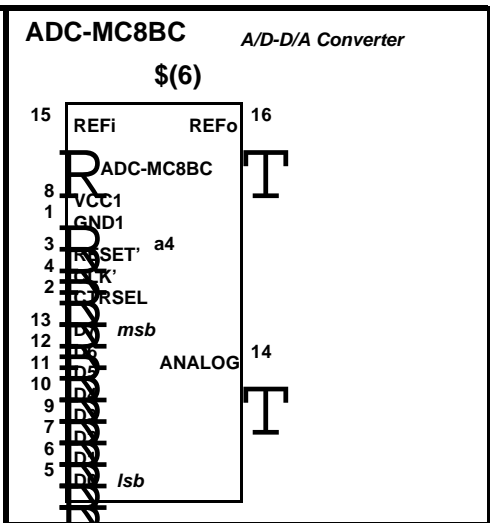
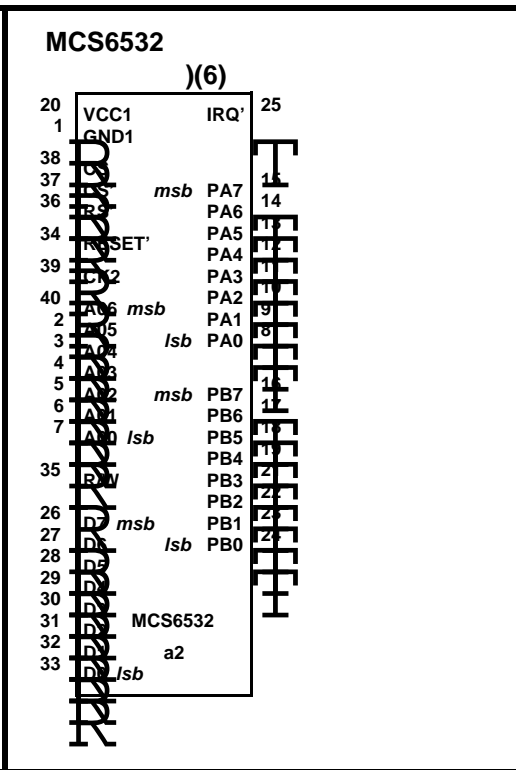
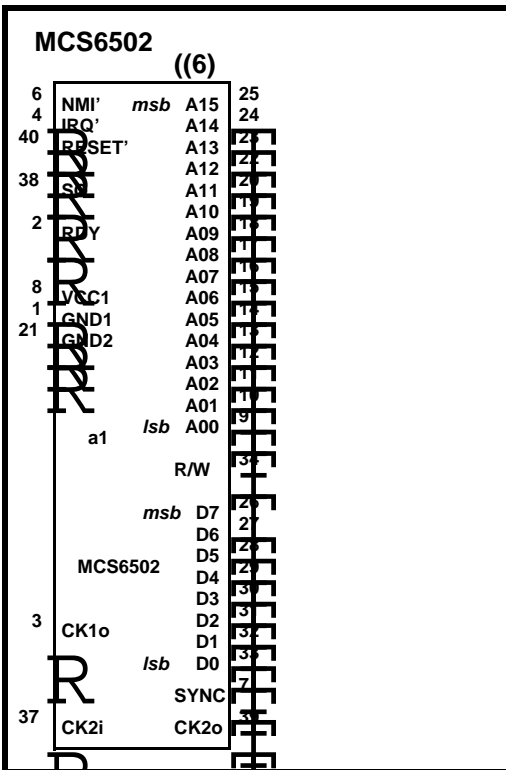
Dual Line Drivers



Differential Inputs	Strobe		OUTPUT
	e	s	
V ge 25mV.	L/H	L/H	H
V < abs(25mV)	L/H	L	H
	L	L/H	H
	H	H	UnKnown
V le -25mV	L/H	L	H
	L	L/H	H
	H	H	L

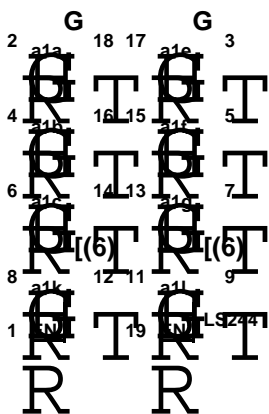


Logic Inputs	Strobe			o	OUT
	IN	a	e		
L/H	L/H	L	L/H	H	H
L/H	L/H	L/H	L	H	H
L	L/H	H	H	L	H
L/H	L	H	H	L	H
H	H	H	H	H	L



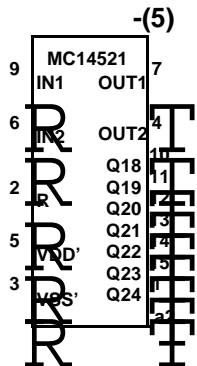
LS244

Octal Buffer/
Drive-receivers



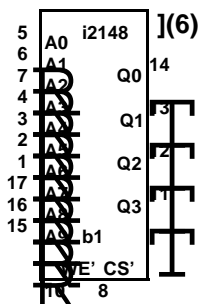
MC14521

24-stage Frequency
Divider



i2114, i2148

1Kx4 Ram



LS378 (SN74LS378)

Hex D-registers

