N151,LS151, S151 N251,LS251, S251

1 of 8 Multiplexor

- S4,S2,S1=000 selects D0
- Tpd S to Y=38.50, 20
- 151
- S4,S2,S1=001 selects D1
- Tpd S to W'=30.39, 16.5
- 251
- S4,S2,S1=010 selects D2
- Tpd D to Y=27.32, 13.5
- 16.5
- S4,S2,S1=100 selects D4
- Tpd D to W'=14.21, 8
- 17
- S4,S2,S1=111 selects D7
- Tpd E to Y=33.42, 20
- 14.5
- Tpd E to W'=23.31, 14.5
- 23

251 has Tri State Outputs

- D0 is the Most Significant bit, D7 is the Least Significant bit

N153,LS153, LS253(AM74LS253), S153, S253(AM74S253)

Dual 1 of 4 multiplexors

- S2,S1=00 selects X0(Y0)
- Tpd S to O=34,38,30, 20
- 10,20
- S2,S1=01 selects X1(Y1)
- Tpd Data to O=23,26,15, 10,10.5
- S2,S1=10 selects X2(Y2)
- Tpd E to O=30,32,25, 16.5,23
- S2,S1=11 selects X3(Y3)

X0/Y0 is the Most Significant bit, X3/Y3 is the Least Significant bit

N155,LS155

Dual to 4 decoders

- S2,S1=00 selects Q0'(R0')
- Tpd S to Q(R)=32,30
- Q0'/R0' is the Most Significant bit, Q3'/R3' is the Least Significant bit
- S2,S1=01 selects Q1'(R1')
- Tpd DQ' to Q=30,27
- S2,S1=10 selects Q2'(R2')
- Tpd DR to R=32,30
- S2,S1=11 selects Q3'(R3')
- Tpd E to Q(R)=27,30

N157,LS157, S157, S257

Quad 2 to 1 multiplexors (non inverting outputs)

- SB=0 selects D
- Tpd SB to Q=27,27, 16.5,16.5
- D0/B0/Q0 is the Most Significant bit, D3/B3/Q3 is the Least Significant bit
- SB=1 selects B
- Tpd E' to Q=21,21, 14,23
- Tpd D/B to Q=14,14, 8.5,8.5

LS158, S158, S258

Quad 2 to 1 multiplexors (inverting outputs)

- SB=0 selects D
- Tpd SB to Q'=24, 13.2
- D0/B0/Q0' is the Most Significant bit, D3/B3/Q3' is the Least Significant bit
- SB=1 selects B
- Tpd E' to Q'=18, 13.2
- Tpd D to Q'=12, 7
9 bit ODD/EVEN parity generator/checker

EVI and OVI are cascading inputs

Arithmetic Logic Unit

Lookahead carry generator

32 by 8 PROM

Synchronous Up/Down Counters with Mode Control

Synchronous Up/Down Counters with Dual clock

Address Access=50,50,30,30
Enable Access=50,50
### 4 bit Bidirectional shift register

- **S2** and **S1** operation:
  - **H H** load
  - **L H** shift right (H1 gets H0)
  - **H L** shift left (H0 gets H1)
  - **L L** do nothing

Clear is asynchronous
- **D0/H0** is the MostSignificant bit
- **D3/H3** is the LeastSignificant bit

16 by 5 FIFO Memory

**See catalog for timing**

### Octal D-Flip-Flop

- **Tpd CK** to **Q** = 30
- **Tpd CL'** to **Q** = 30

### 4 bits Arithmetic Logic Unit

- **Tpd D/E** to **H** = 24, 24, 18.5
- **Tpd CI** to **H** = 21, 24, 20.5
- **Data setup = 20, 20, 6**
- **Mode setup = 30, 30, 12**
- **All holds = 0, 0, 4**
- **Min width Clock = 20, 20, 9**
- **Min width Clear = 20, 20, 14**
- **Min Clear Inactive = 20, 20, 10**

**See catalog for timing**

### Four Bit adder

- **Tpd D/E** to **H** = 24, 24, 20
- **Tpd CI** to **H** = 21, 24, 20
- **Tpd CI** to **CO** = 16, 17, 12.5
- **Tpd D/E** to **CO** = 16, 17, 13.5

**D0/E0/H0** is the MostSignificant bit
- **D3/E3/H3** is the LeastSignificant bit

**CI** is the Carry Input
- **CO** is the Carry Output

### Quad 2 input multiplexor/register

- **SB = 0** selects **D** inputs
- **SB = 1** selects **B** inputs

- **Clock on negative transition**

**Tpd CK’** to **Q** = 32
- **Min width CK’ = 20**
- **Data Set-up = 15**
- **Data Hold = 5**
- **SB setup = 25**
- **SB Hold = 0**

**D0/B0/Q0** is the MostSignificant bit
- **D3/B3/Q3** is the LeastSignificant bit
2115 and 93415 are OC output
2125 and 93425 are tristate outputs

2115, 2125, 93415, 93425 are tristate outputs
2115, 2125, 93415, 93425 are tristate outputs

Address Access=70,45
Chip Select=40,30
Write pulse min=35,50
Data Setup=5,5 Hold=5,5
Address Setup=15,5 Hold=5,5

See data sheets for more information on write cycles

Address Access=35
Chip Select=17
Sense Amp Recovery=35
Write pulse min=25
Address Setup/Hold=0

Data stable prior to l to h transition on WRITE=25

Address Access=50, 40
Enable Access=25,25

Note pin numbers are not the same as in catalogue

See data sheet for timing spec

Note pin numbers are not all same as in catalogue

See Data Sheet

Note pin numbers are not all same as in catalogue

See TI Databook Page 7-437

For Power Connection
Not Needed on S-board

See Data Sheet for timing specs

See Data Sheet for timing specs
**Note Pin#8 is grounded**

**Note** it is staffed in the middle of a 20 pins position on S-board so to avoid GND and VCC

Added the following subgroups in your drawings if you do not want the trace-wire of GND & VCC to be CUT:

```
GND 10 20
VCC 10 20
```

**Tpd A’s to Q= 50**

**Tpd CS’ to Q=30**