PDP EtherNet Network Connection

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General Description

The PDP-11/Ethernet interface module will enable the connection of DEC PDP-11/34 and 11/39 series computers and any other machine utilizing a DD11-PK backplane to the EtherNet communications network. The unit may also be used in computers with signals on connectors "C, D, E, and F" compatible with the DK11-PK backplane. The interface is be a single module plugged into the mainframe, deriving power from the mainframe and requiring only the ethernet transceiver and cable as external devices.

Caveat: The module expects to find +15 volts at 125 mA available at Pin U1 of connector "C" or alternately at Pin R1 of connector "A"! The DEC machine used must have this voltage available.

Caveat: There are early versions of PDP machines in which the fan assemblies protrude into the space above connector "A". The interface module will not physically fit into these machines.

Physical Description

The circuit board is a hex module approximately 8.5 by 15.75 inches with six connectors for insertion into connectors A,B,C,D,E, and F of the backplane. An outer edge ribbon connector provides access via a ribbon cable to a PDP-11 bulkhead connector and to the Ethernet transceiver cable. A DIP Switch must be set to define the unit Ethernet address assigned at the time of installation. A DEC plug-in PC module must also be installed to define the Bus Grant level, from 4 to 7, and to provide continuity for unused Grant strings.

The wire from C1A to C1B on the backplane of the slot into which the module is to be installed must be removed for proper operation.

Electrical Description

The interface communicates via the PDP Unibus with the CPU for control and status and with the memory for DMA type data transfers. Control and status information transfer is CPU initiated by addressing pseudo-memory locations within the interface hardware. Addresses currently defined are asssigned compatible with the 9700 structure. Data transfers to/from memory are interface initiated when the I/O channels have been enabled via the control words and data is available/needed by the channel. Transfers occur on a Unibus cycle steal basis. Operation is full duplex allowing the PDP-11 to send messages to itself for diagnostic purposes.

Output data. The location of the output buffer in the first 64K of real memory and the two's complement of the buffer length are transferred by the CPU to the pseudo-memory locations in the interface and the output is enabled by setting an enable bit in the control register. The interface will then initiate access requests for data from memory and start filling its FIFO buffer. When the net is quiet, the data will be prefixed by a single 'one', phase encoded and shifted to the net. The process continues until the buffer length counter overflows; the FIFO is then flushed, the CRC is appended and output stops.

If a collision is detected during the transmission period, the interface will jam the net, output will cease, and an interrupt request with vector 410_B will be generated. The interrupt software routine should generate a random delay count. load the count into the Output Delay Start Register and restart the output. The hardware will decrement the delay count to zero using an asynchronous 43.5 microsecond period clock. On reaching zero and detecting a quiet line, the hardware will retry the transmission. The restart attempts should be made with the maximum random delay period doubled after each aborted attempt. After a maximum number of unsuccessful retries, the tries will cease and the handler will notify the user of an abort.

Input data. The location of the memory input buffer in the first 64K of real memory and the two's complement of the maximum allowable buffer length are transferred by the CPU to the pseudo-

memory locations in the interface. When enabled, the interface will check the destination byte of all pups on the net and, if an address recognition occurres, it will begin accumulating sixteen bit data words in the input FIFO. Data in the FIFO will cause access requests to be generated and data will be transferred to memory. Accumulation will continue until the end of the pup, CRC will be checked, the FIFO will be flushed and if enabled, an interrupt requested. Setting a promiscuous bit in the control word will cause any pup on the net to be recognized and input.

Programming

Hardware devices are assigned pseudo-memory addresses in the upper 8K of memory. The Ethernet interface normally uses a block of eight floating word addresses, 760020 to 760036, used for communications equipment. A switch on the module, shown in Figure 1 (PDP11SW.sil), allows setting the starting address over the range of 760000 to 777760. The addresses are assigned as follows:

|	
760020_B	Load output word count.
760022_B	Load output buffer location.
760024_B	Load/read output control and status.
760026_B	Load output start delay.
760030_B	Load/read input word count.
760032_B	Load input buffer location.
760034_B	Load/read input control and status.
760036_B	Read device address.

Output word count.

B_{15} B_9 B_0

| 2's Comp |
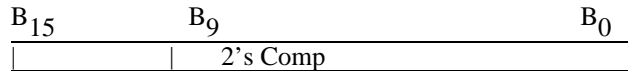
CRC is generated by the hardware and is not included in the byte count.

Output buffer location.

B_{15} B_0

| Address |

Output control and status word.

B_{15} $B_7 B_6$ B_0
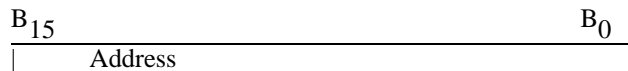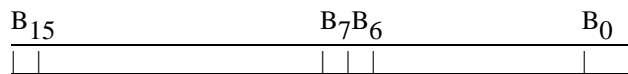
B_{15} Error: Indicates that a collision occurred and the data was not transmitted or an output underrun occurred.
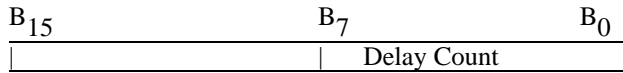
B_7 Done: Indicates that the previous operation was successfully completed or aborted.

B_6 Interrupt Enable: When set, the interface will generate an interrupt request when B_7(Done) is set.
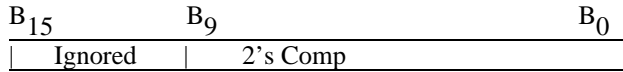
B5, B4 CAVEAT, not implemented! DMA interface does not use extension bits; buffer locations must be in the first 64K of real memory.

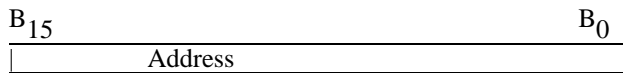B_0 Enable: When set by the CPU, enables an output operation.

Output start delay.

```
B15                          B7                    B0
|                              |   Delay Count        |
```

Input word count.

```
B15          B9                                 B0
|  Ignored   |   2's Comp                         |
```
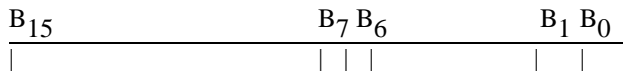
Bits 15 thru 10 are ignored by the hardware during Load Input Word Count. When the residual count is retrieved with Read Input Word Count, the 2's complement is contained in Bits 9 thru 0, *and Bits 15 thru 10 are 0's*.

The CRC is not input to memory but should be included in the word count. If the input count is equal to the expected PUP size without the CRC the word count will cause a buffer overflow error. This may change in the future but that is what the hardware does now.

Input buffer location.

```
B15                                             B0
|        Address                                  |
```

Input control and status word.

```
B15                     B7 B6            B1 B0
|                        |  |  |          |  |  |
```

B_{15} Error: Indicates that the CRC was not correct, a buffer overflow or an overrun occurred during the previous operation.
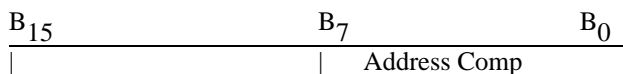
B_7 Done: Indicates that an operation has been completed.

B_6 Interrupt Enable: When set, the interface will generate an interrupt request when B_7(Done) is set.

B1 Promiscuous: When set, the interface will input any packet on the net.

B_0 Enable: When set by the CPU, initiates an input operation.

Device address

```
B15                          B7                    B0
|                              |   Address Comp       |
```

The device address is an eight bit byte wired on the Ethernet module and the complement may be read by the line handler for insertion into the pup as the source address. This is the address used for destination comparison with pups received on the net. *Bits 15 thru 8 are 0's and Bits 7 thru 0 contain the complement of the address*. Not at all clean but it wasn't caught until checkout and there isn't space on the board to correct it. Selection of the device address is shown in Figure 1 (PDP11SW.sil).

When interrupts are requested (enabled), at the termination of output/input operations, the

hardware provides a vector to a pair of words for interrupt processing. The vectors used are the vectors above the communications equipment. (Vectors may be modified by cutting the etch between E3 and E4 and adding wire jumpers on the module starting the interrupts at any location from 000_B to 760_B.) The vectors are:

Output Complete	400_B
Input Complete	404_B
Collision Occurred	410_B

The jumper locations for selection of the interrupt locations are shown in Figure 1 (PDP11SW.sil).

Installation

The module is provided with a level 5 priority jumper plug in a socket in location A15 (may be soldered in). Priority level may be changed by replacing the plug with the desired level plug. Plugs are available from DEC as:

Level 4 P/N 5408776-00
Level 5 P/N 5408778-00
Level 6 P/N 5408780-00
Level 7 P/N 5408782-00

Care should be taken to note the pin orientation with Pin 1 rotated from the IC Pin 1. Pin 1 is not marked on the DEC plug but is the unused pin next to the priority level designation.

The interrupt locations, device address, and I/O address block location should be set by jumpers and switches shown in Figure 1 (PDP11SW.sil).

The backplane jumper from C1A to C1B must be removed from the connector of the slot used by the module.
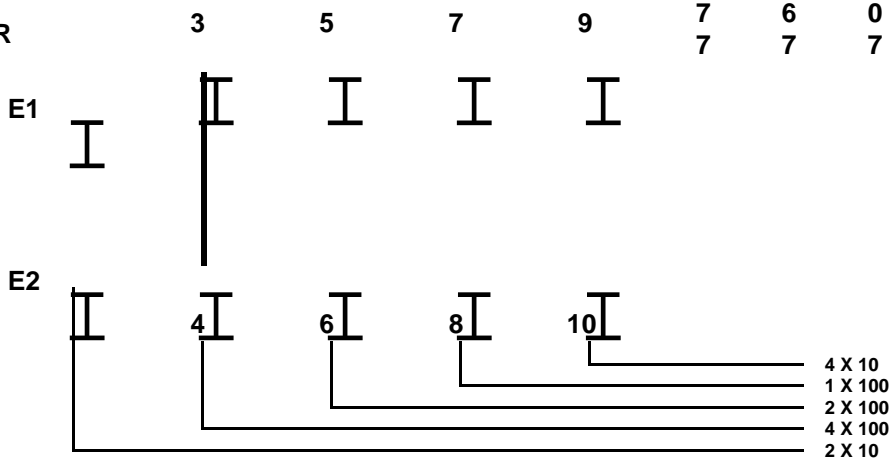
A24

I/O STARTING ADDRESS
RANGES FROM
760000 TO 777760

PUSH OPEN SIDE FOR A '1'
PUSH NUMBER SIDE FOR A '0'

O
P
E
N

1 1
2 2
3 3
4 4
5 5
6 6
7 7
8 8
9 9

111	11X	XXX	XXX	XX0	000
7	6	0	0	0	0
7	7	7	7	6	0
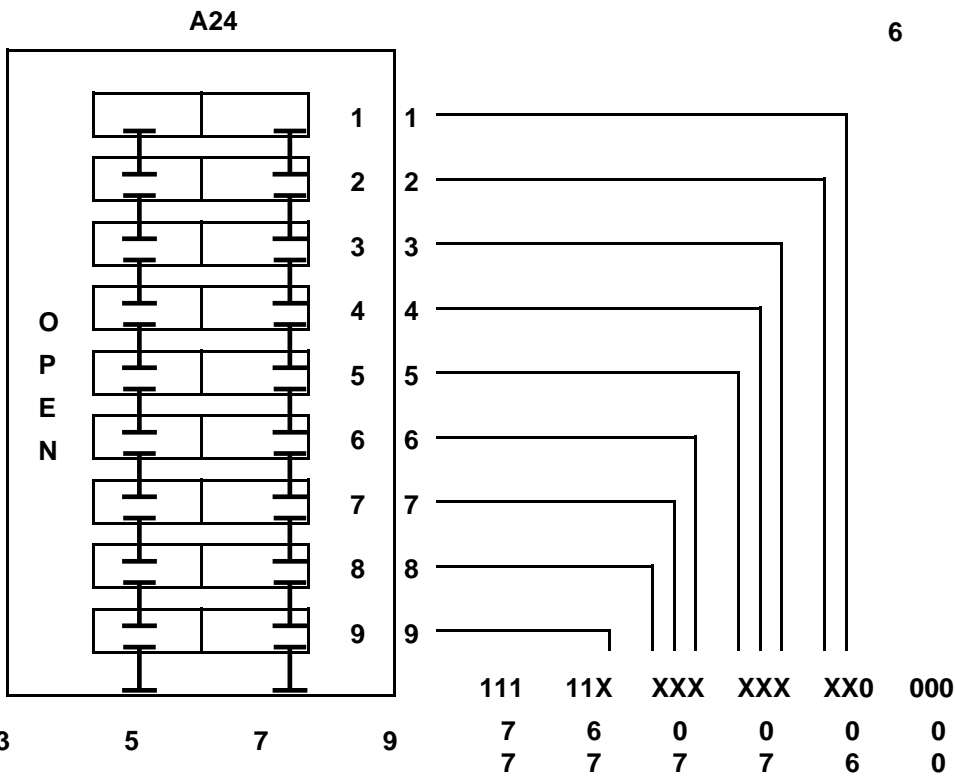
ETCH JUMPER SHOWN FOR

INTERRUPT LOCATIONS

    400
    404
    410

TO MODIFY, CUT ETCH
AND ADD JUMPERS
AS REQUIRED

3 5 7 9

E1

E2

4 6 8 10

4 X 10
1 X 100
2 X 100
4 X 100
2 X 10

UNIT ADDRESS

MSB   LSB

A87

PUSH NUMBER SIDE FOR A '1'
PUSH OPEN SIDE FOR A '0'

O
P
E
N

1 1
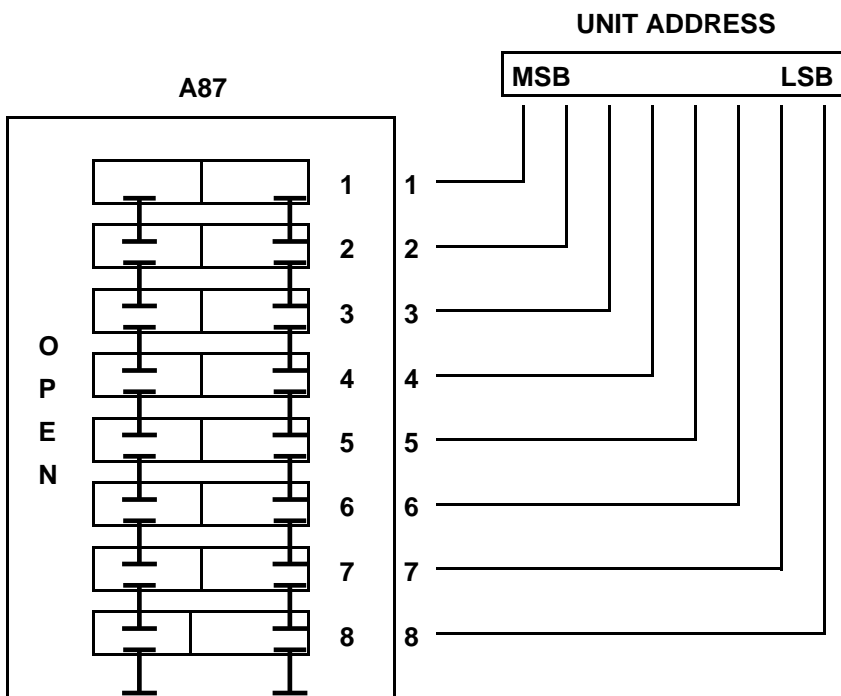2 2
3 3
4 4
5 5
6 6
7 7
8 8

FIGURE 1.   PDP11 ETHERNET NETWORK INTERFACE SWITCH SETTINGS
Filed on: PDP11SW.sil