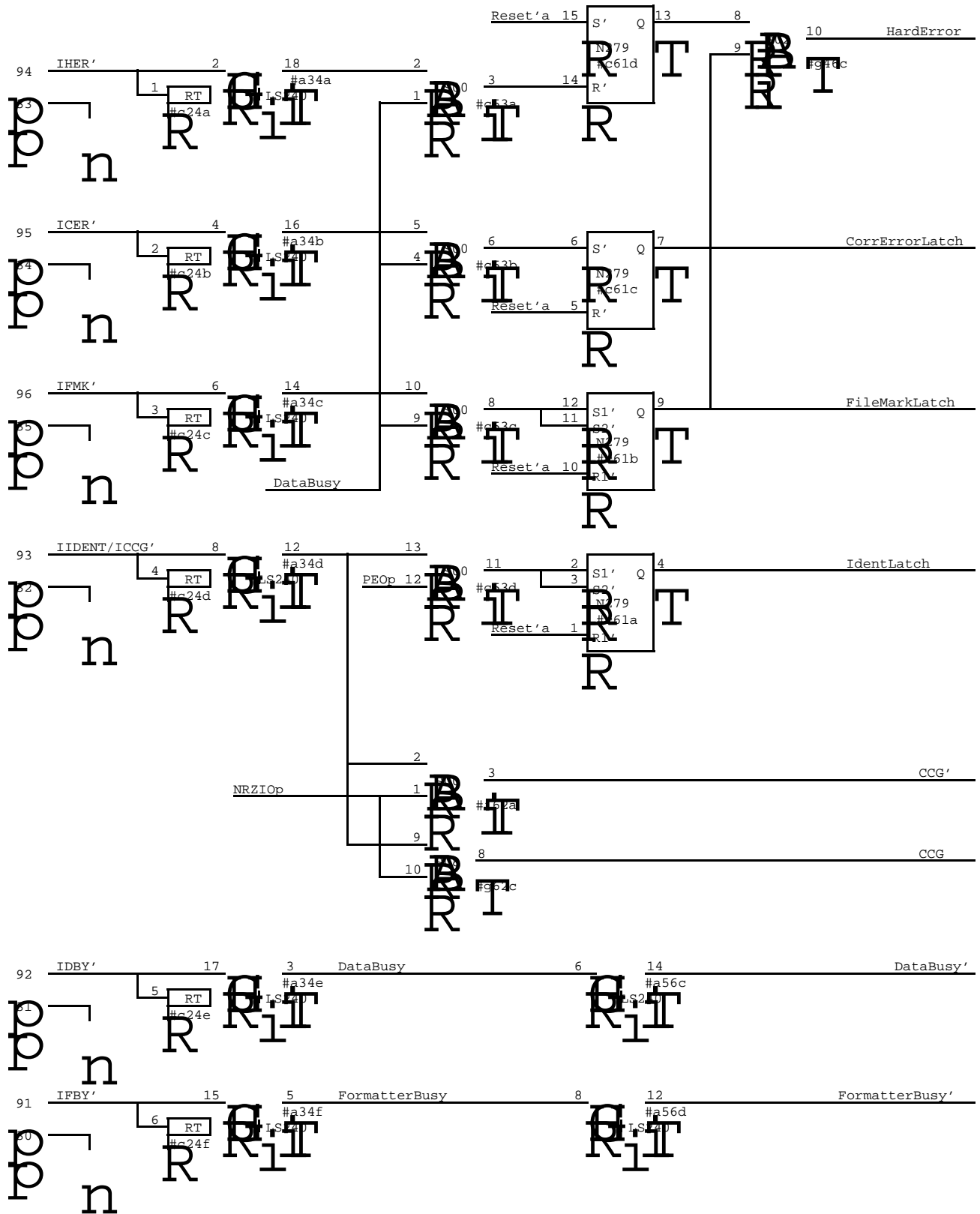
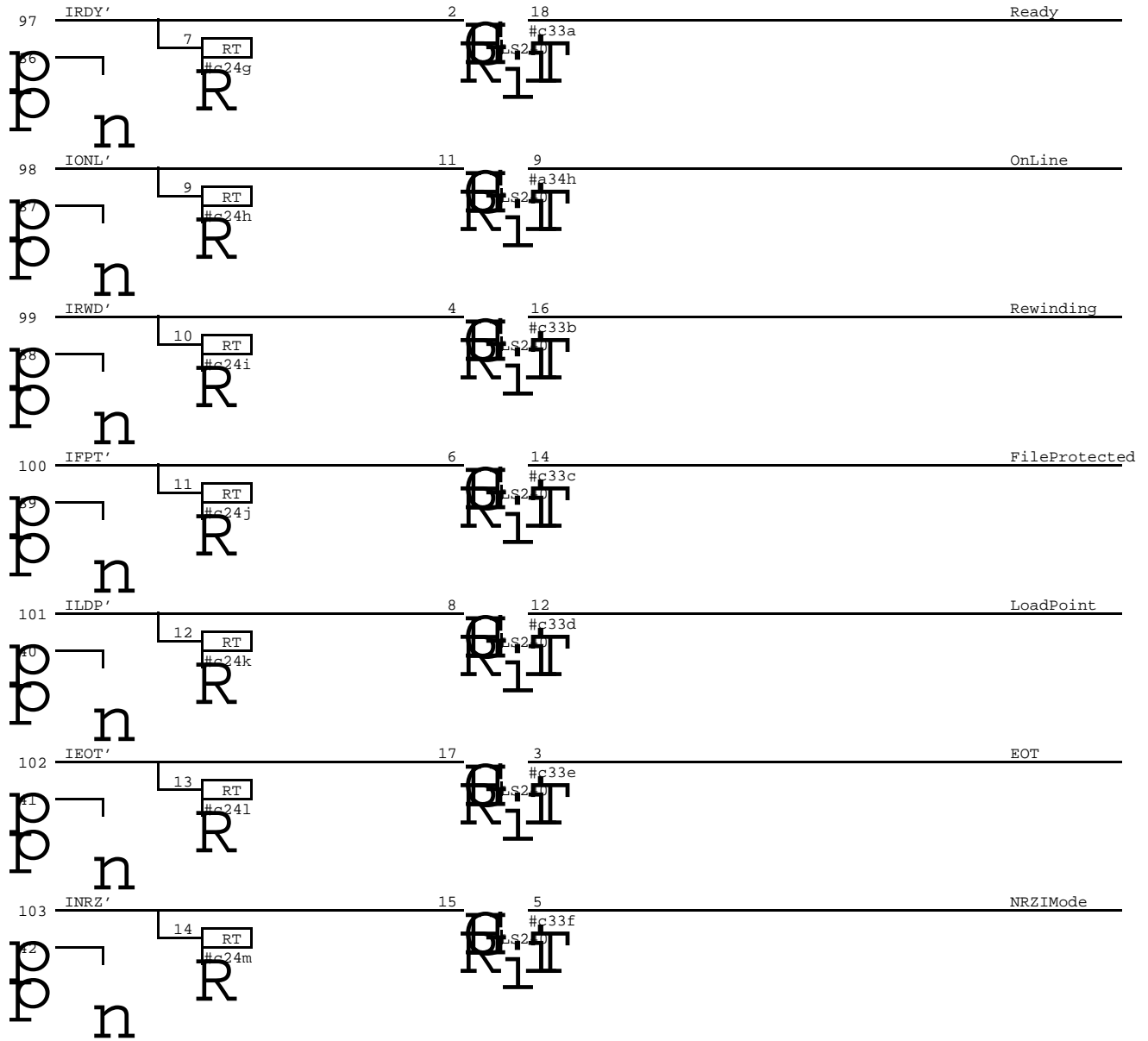


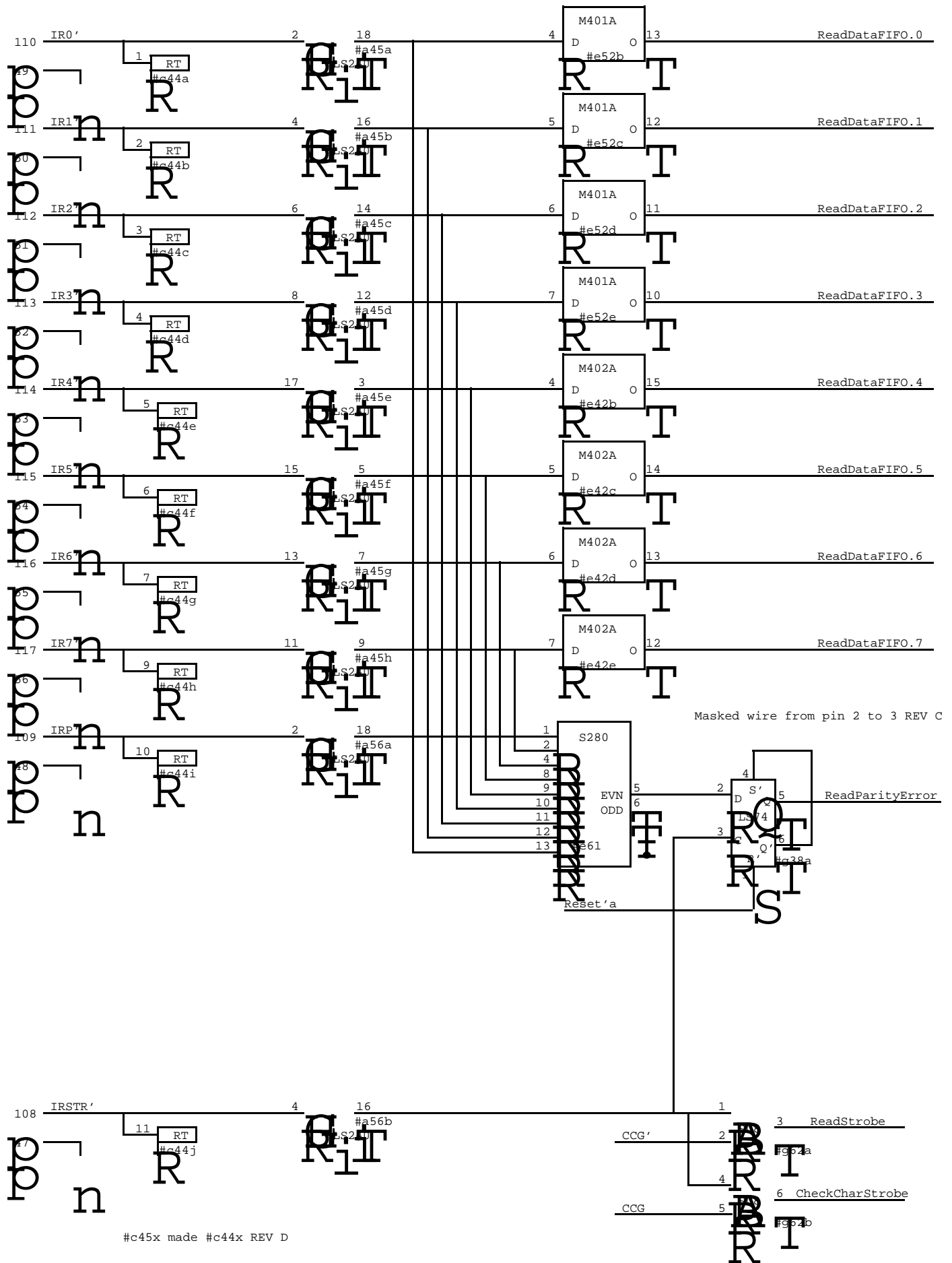
A L T O D U A L D E N S I T Y
 T A P E C O N T R O L L E R
 D D T a p e

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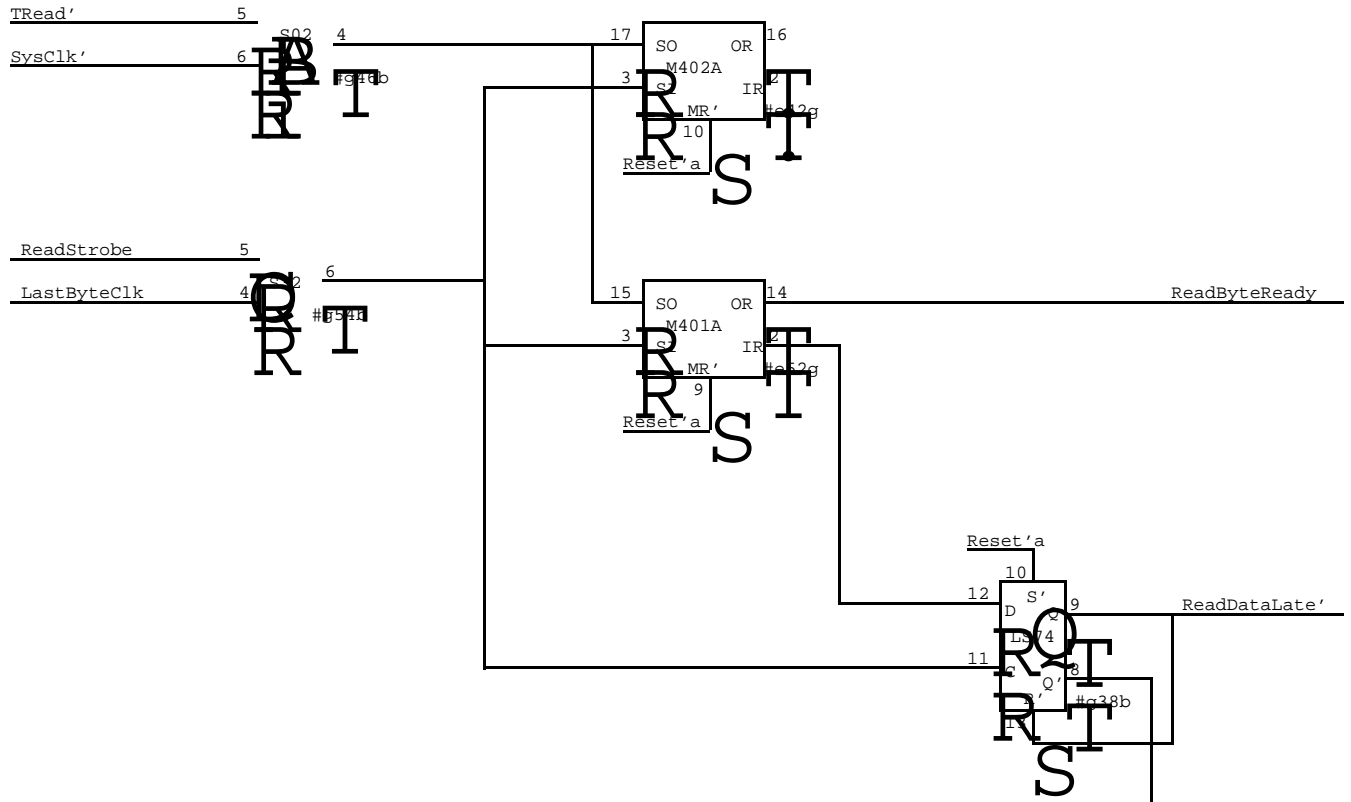
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Formatter Status _____	0 1
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Read Data Interface and FIEO _____	0 3
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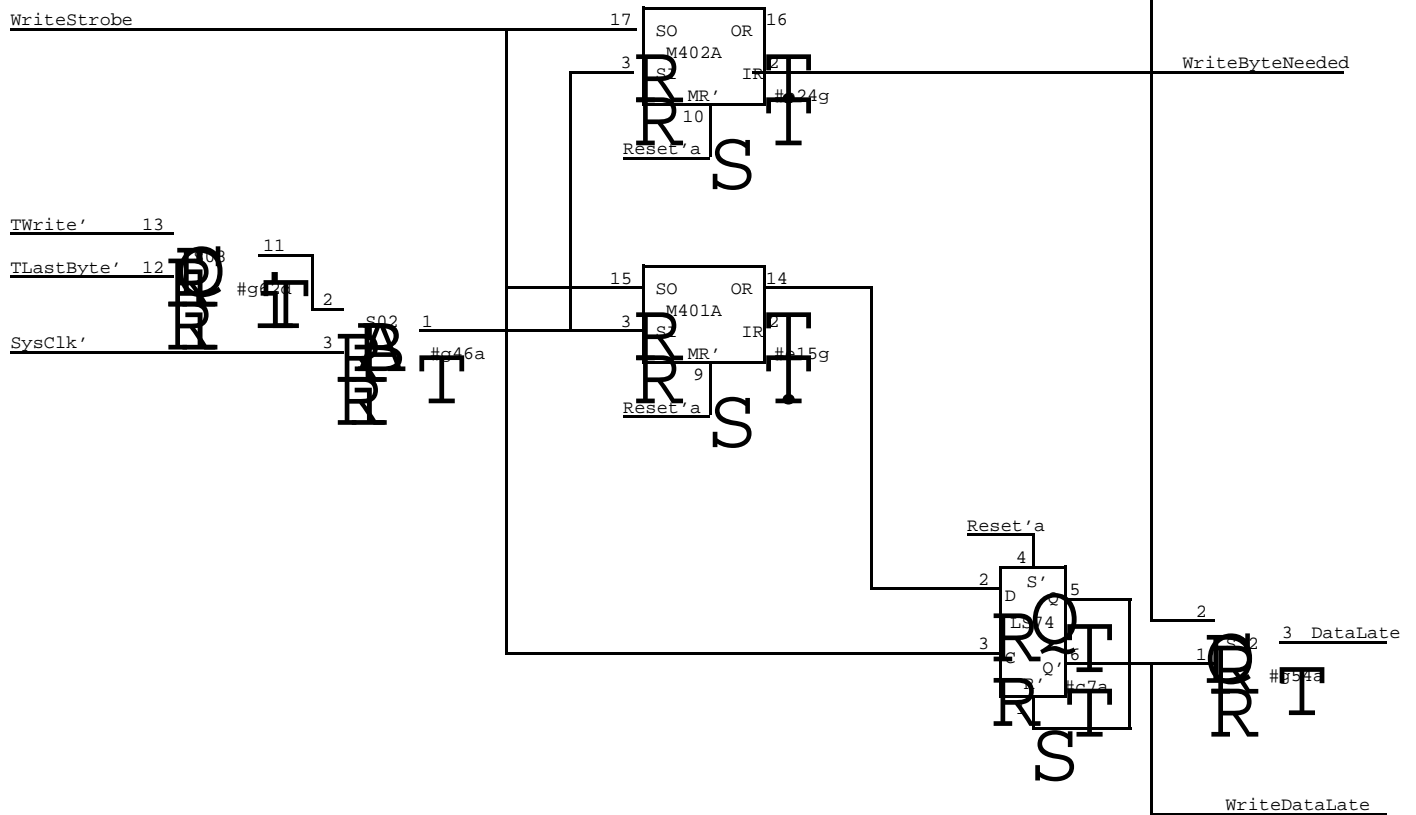




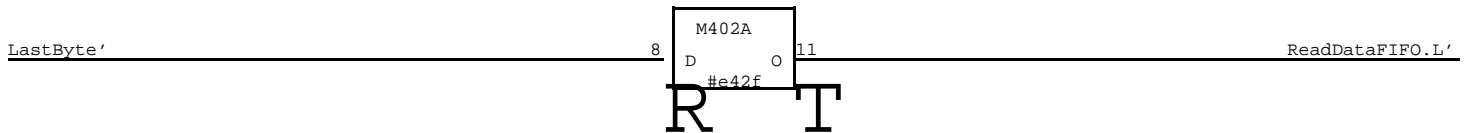
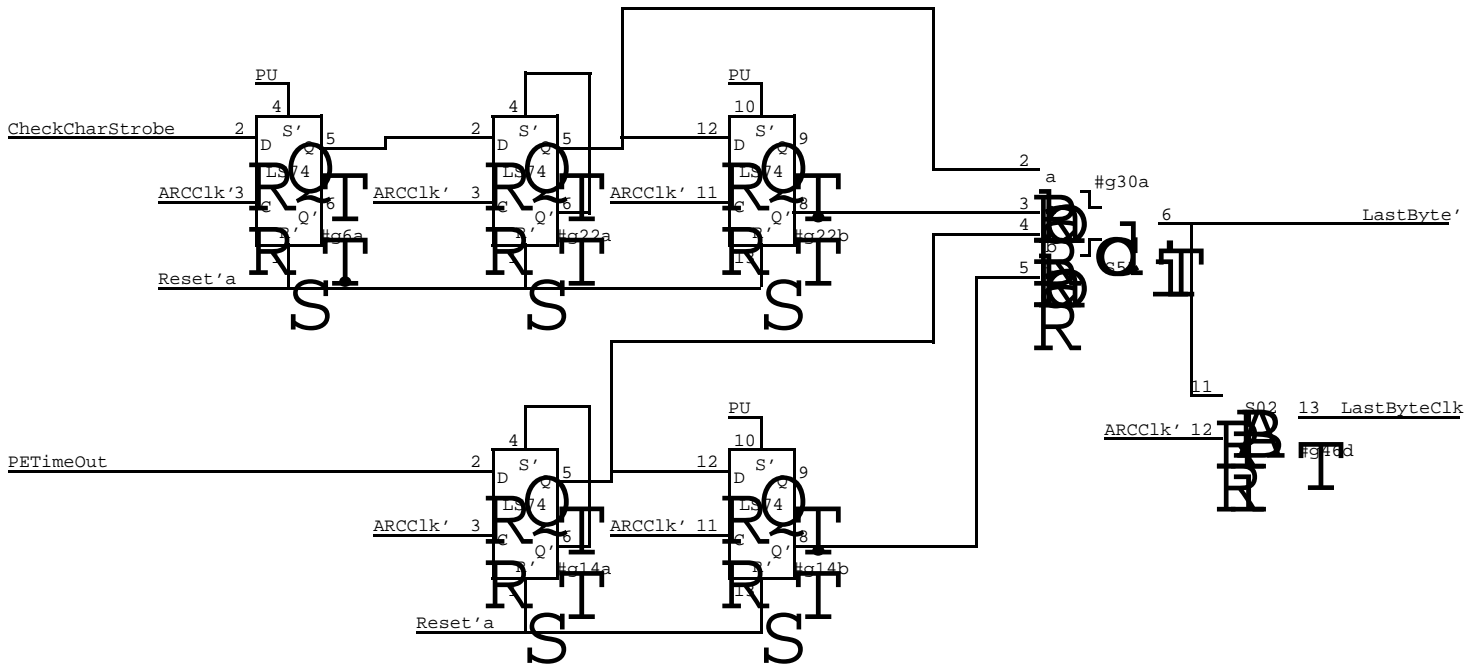
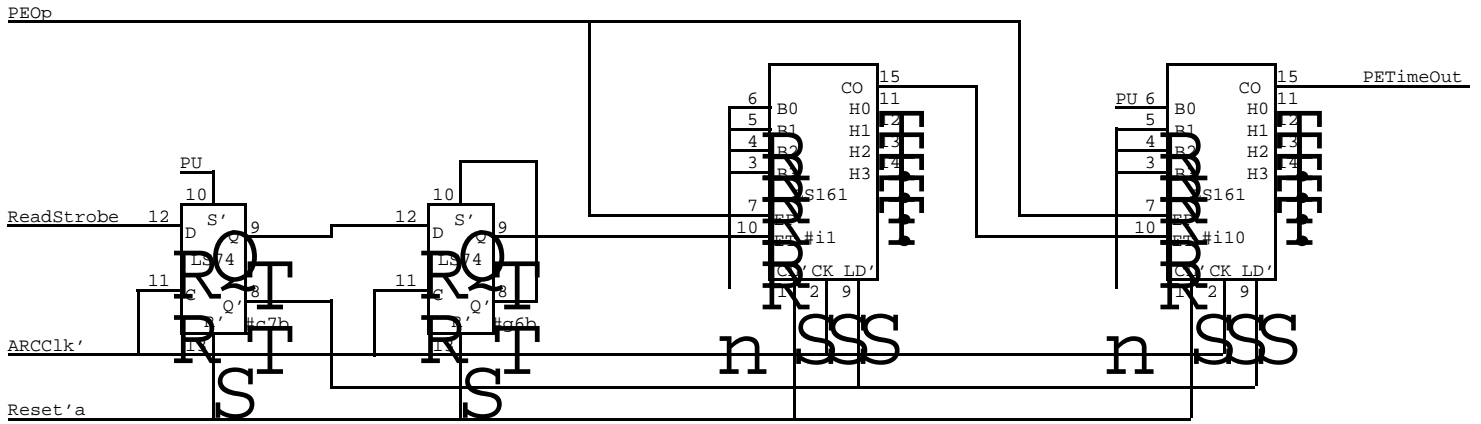
#c45x made #c44x REV D

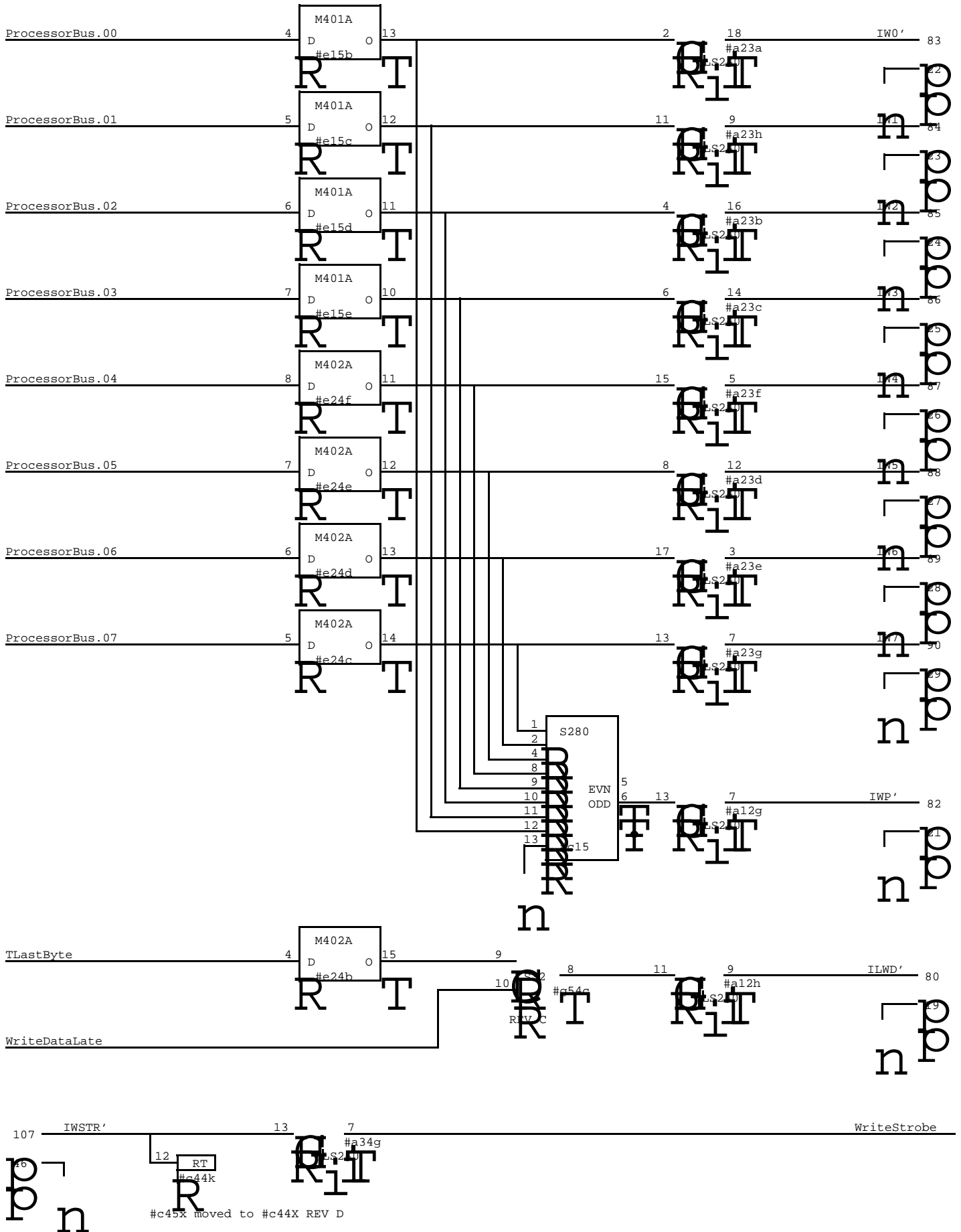


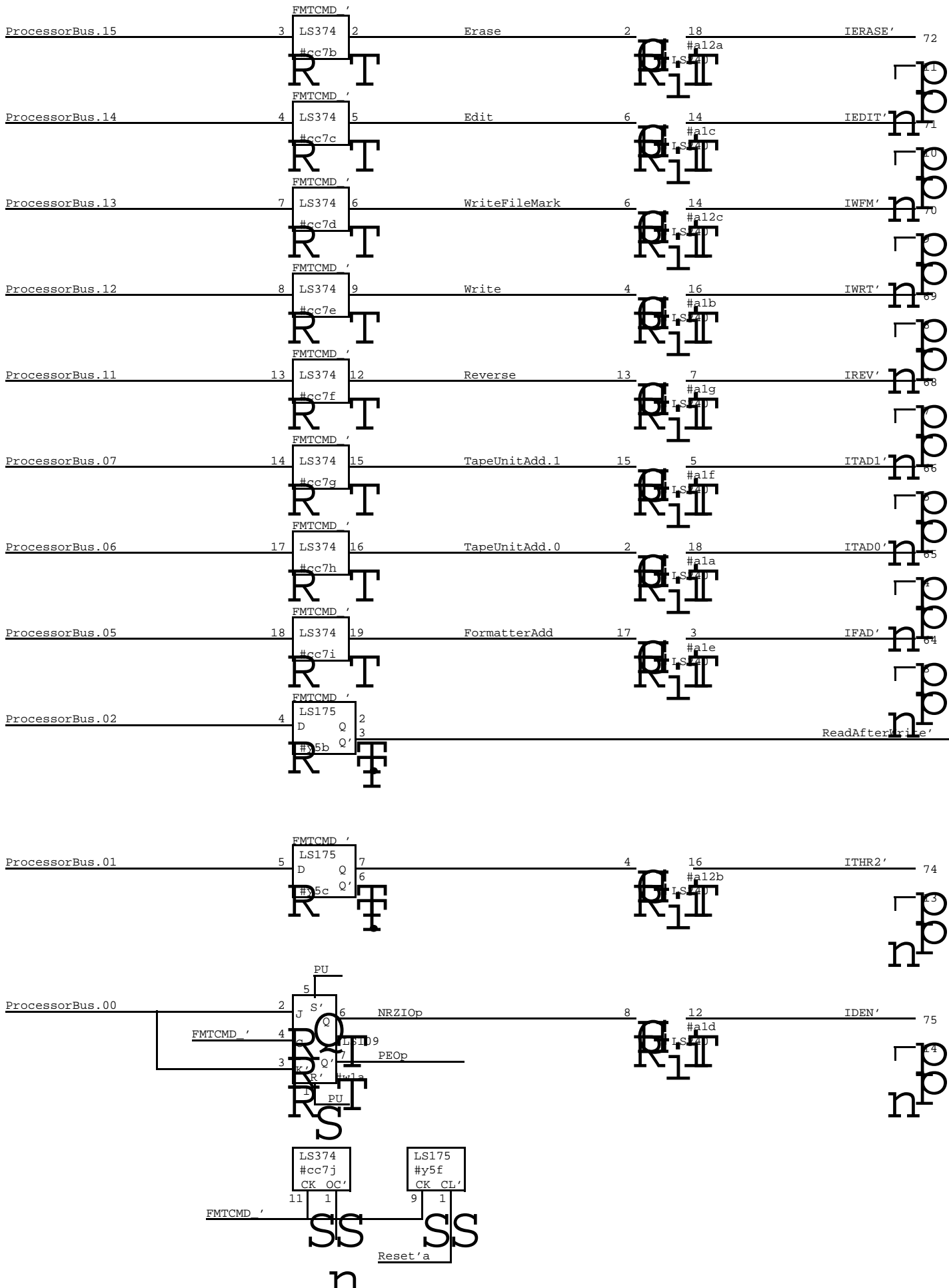
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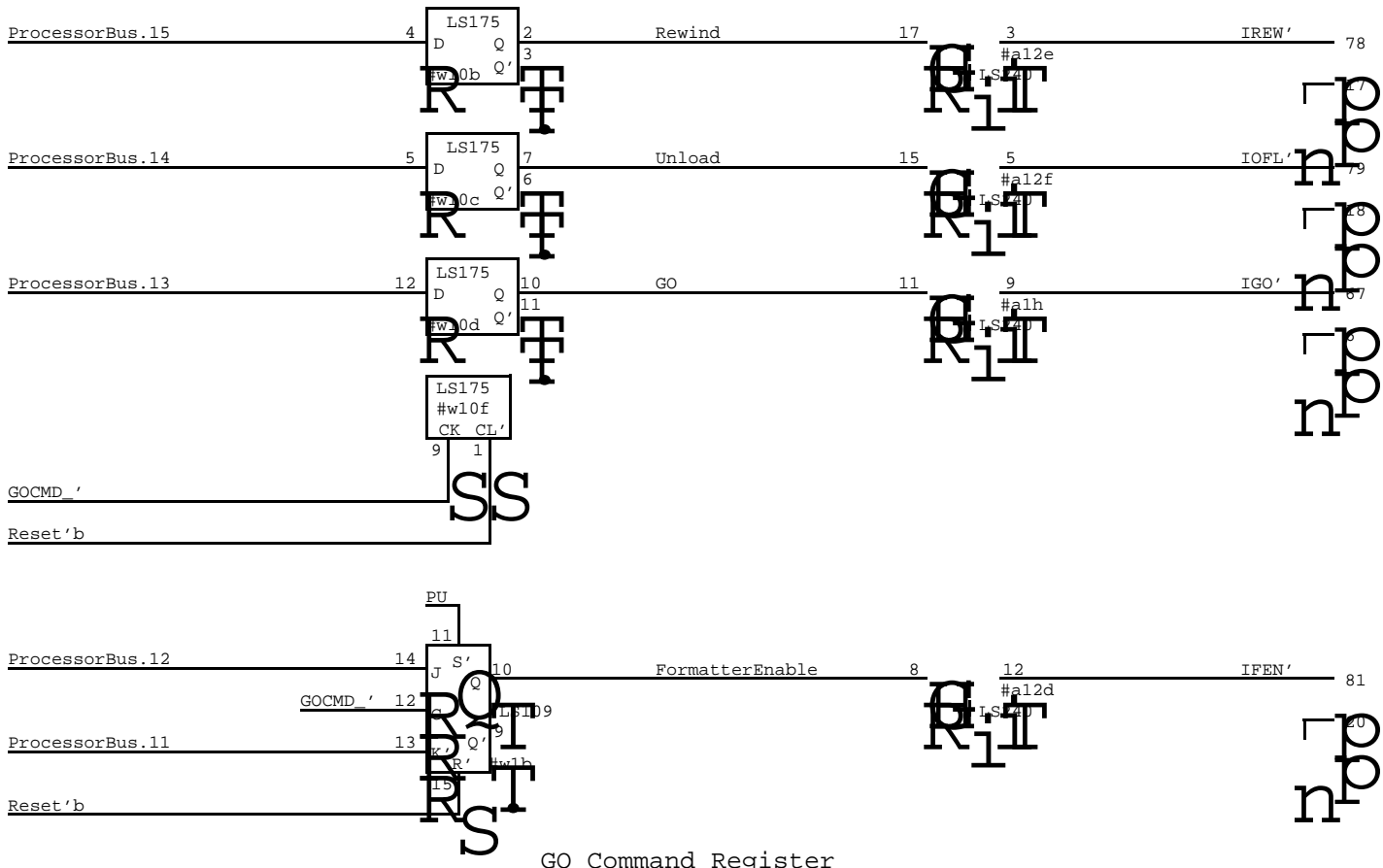


Write FIFO Control









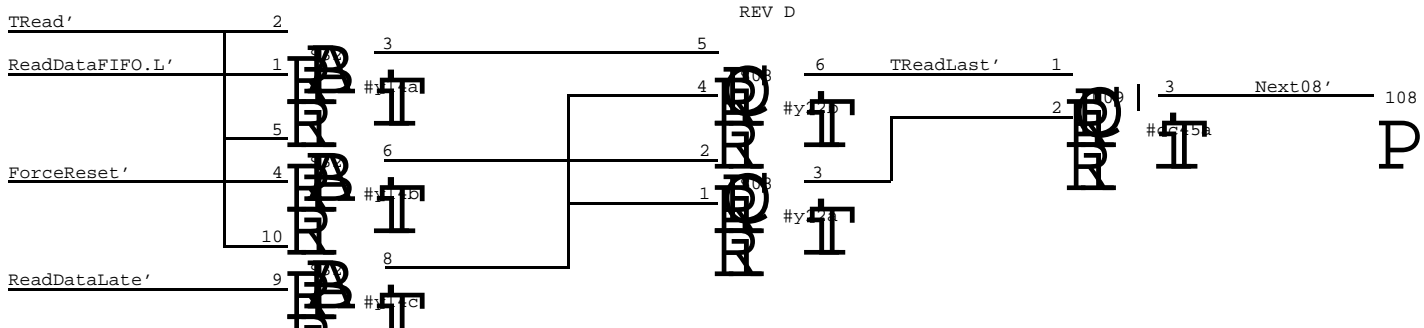
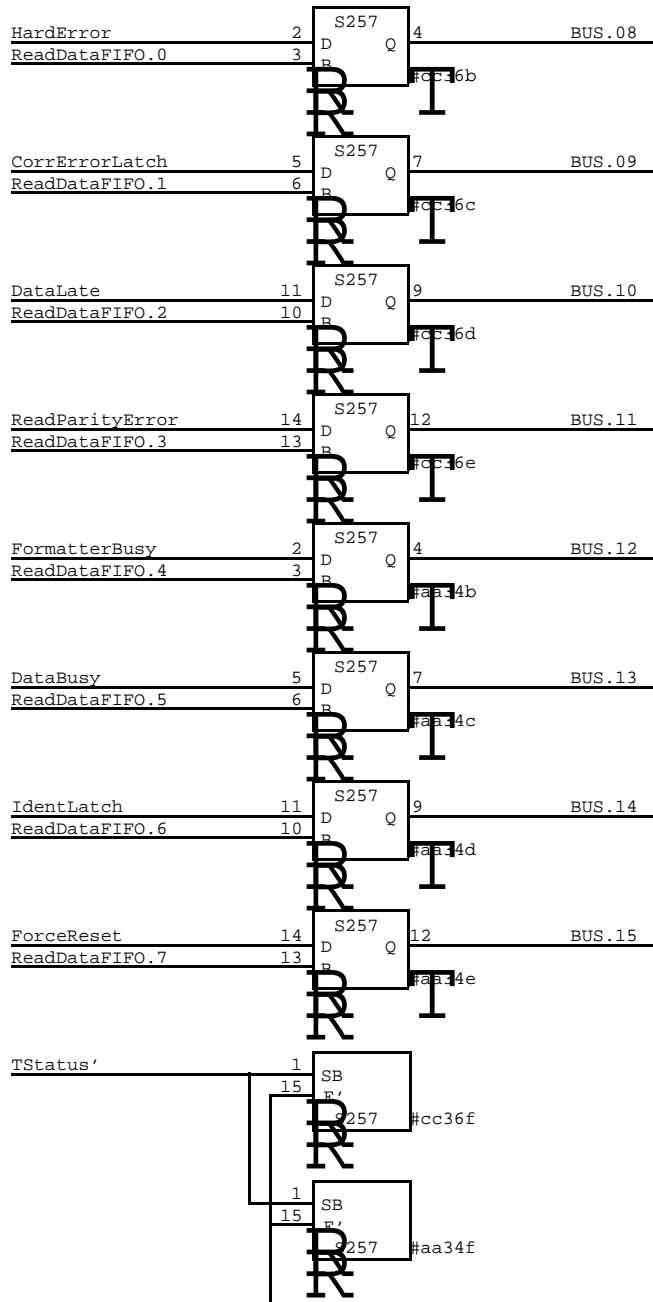
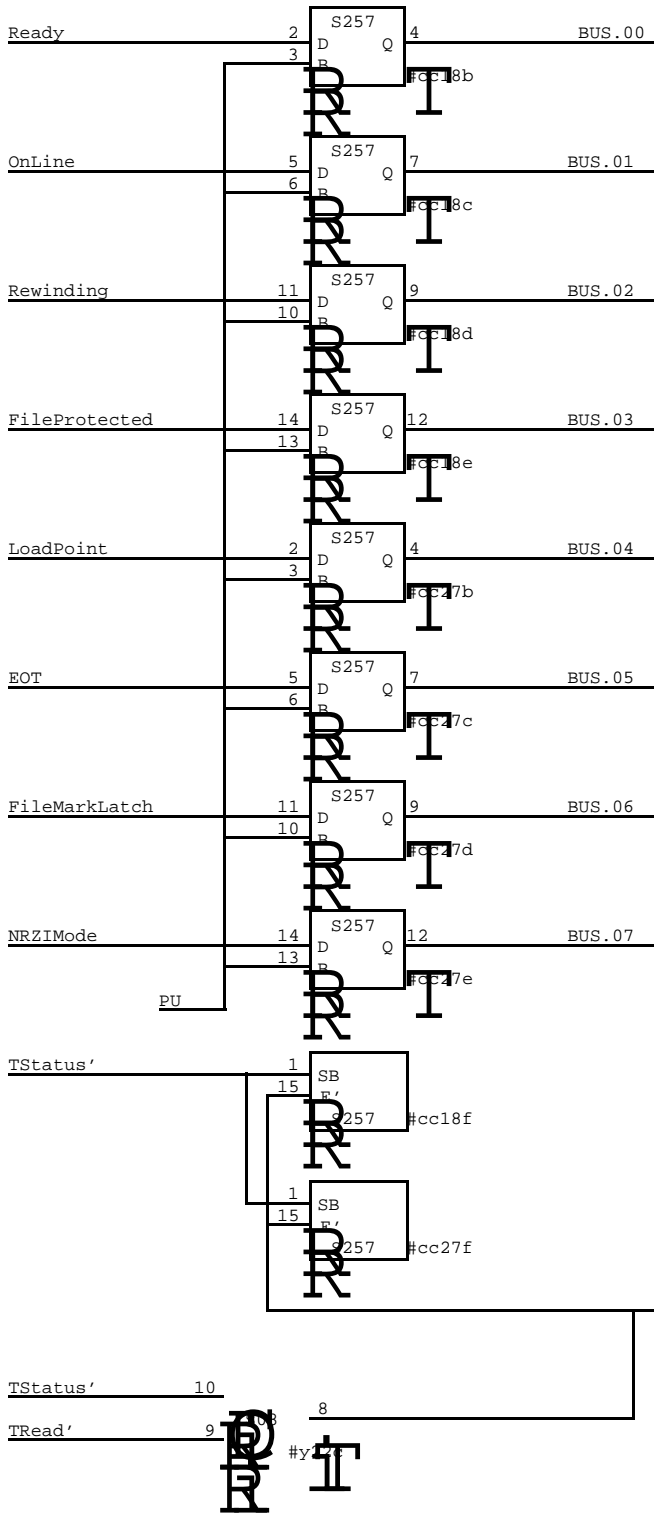
GO Command Register

95	BUS.15	2	18	ProcessorBus.15
				#ee28a
94	BUS.14	4	16	ProcessorBus.14
				#ee28b
93	BUS.13	6	14	ProcessorBus.13
				#ee28c
92	BUS.12	8	12	ProcessorBus.12
				#ee28d
91	BUS.11	17	3	ProcessorBus.11
				#ee28e
90	BUS.10	15	5	ProcessorBus.10
				#ee28f
89	BUS.09	13	7	ProcessorBus.09
				#ee28g
88	BUS.08	11	9	ProcessorBus.08
				#ee28h

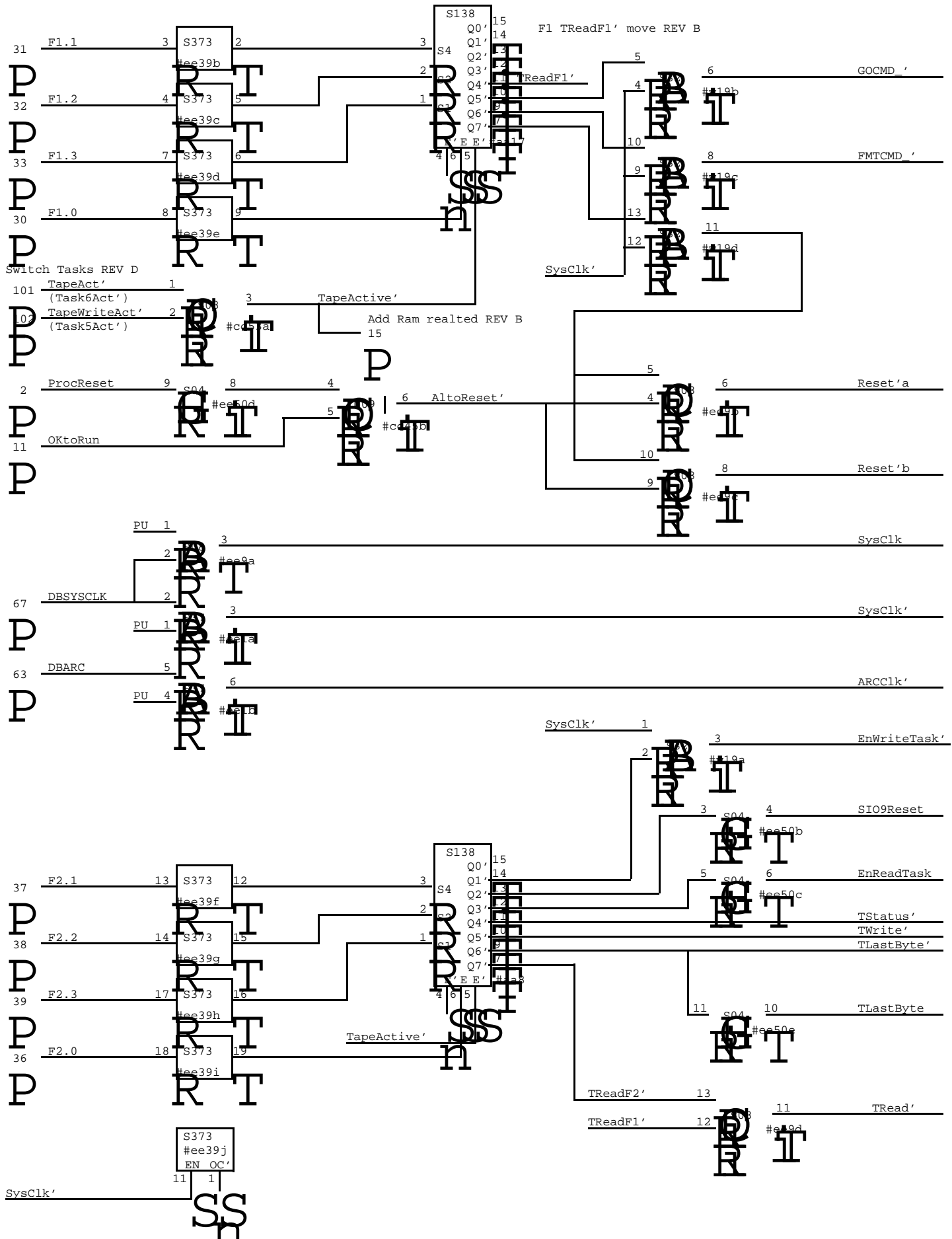
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				#ee17a
86	BUS.06	4	16	ProcessorBus.06
				#ee17b
85	BUS.05	6	14	ProcessorBus.05
				#ee17c
84	BUS.04	8	12	ProcessorBus.04
				#ee17d
83	BUS.03	17	3	ProcessorBus.03
				#ee17e
82	BUS.02	15	5	ProcessorBus.02
				#ee17f
81	BUS.01	13	7	ProcessorBus.01
				#ee17g
80	BUS.00	11	9	ProcessorBus.00
				#ee17h

Alto Bus Interface

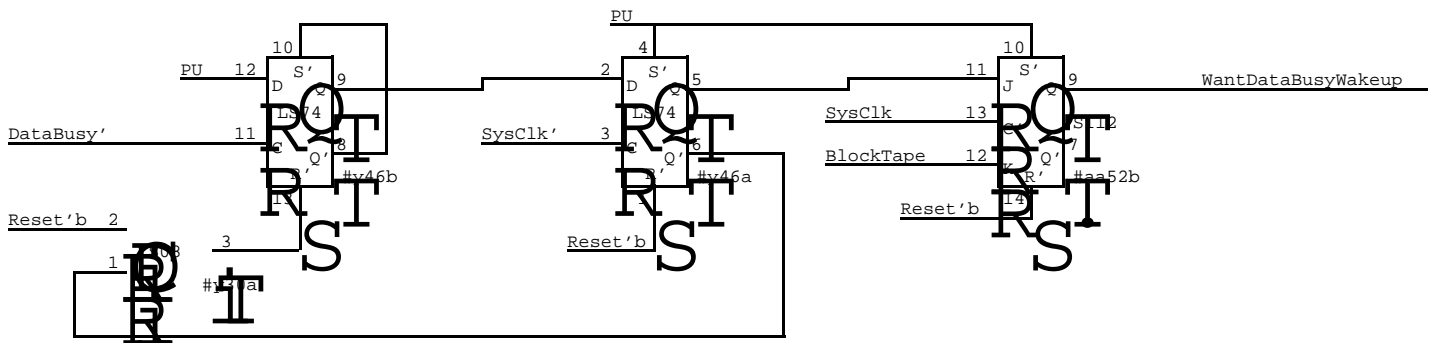
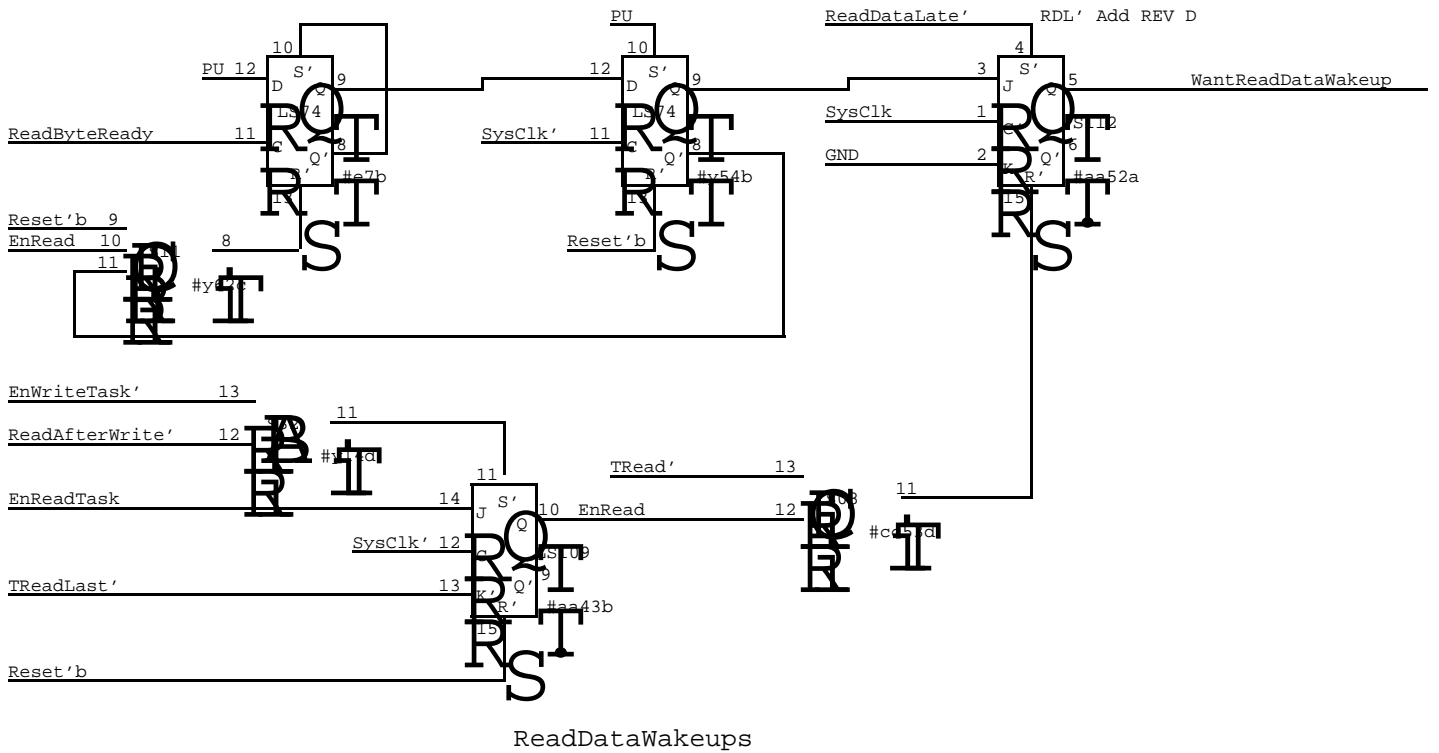
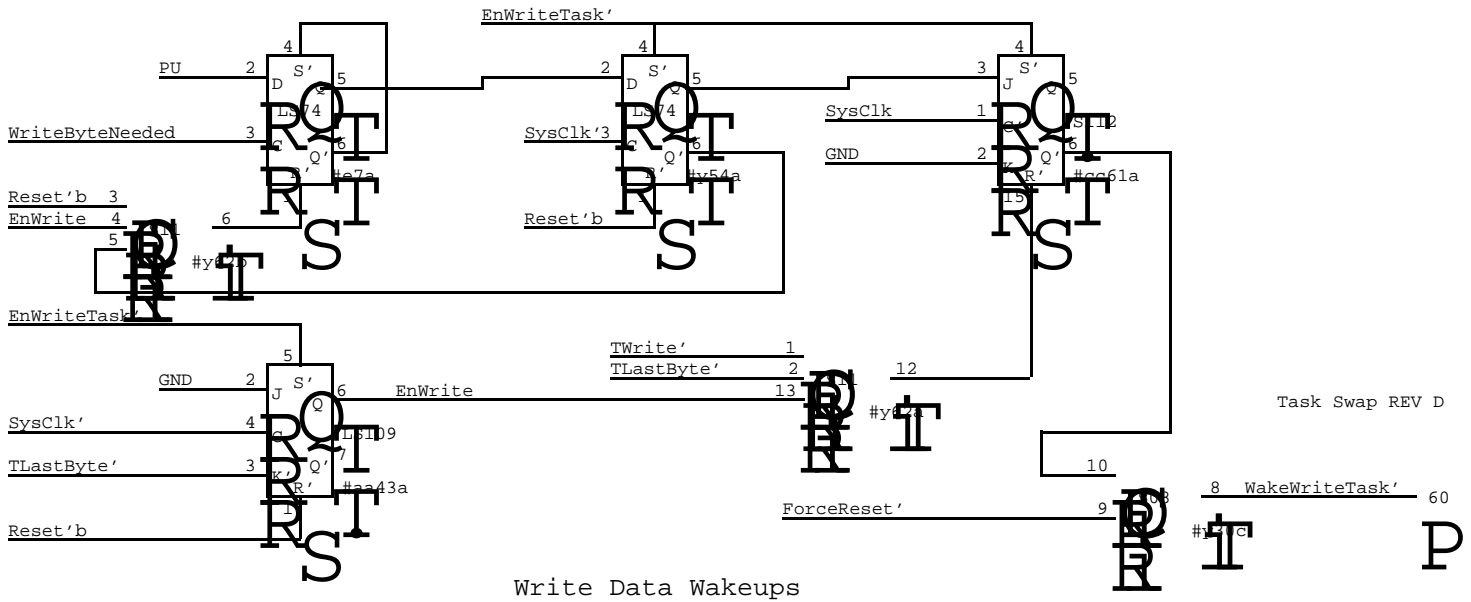
XEROX PARC/CSL	Project DDTape	GO Command Register Alto Bus Interface	File DDTape08.sil	Designer Tim Diebert	Rev D	Date 12/18/80	Page 09
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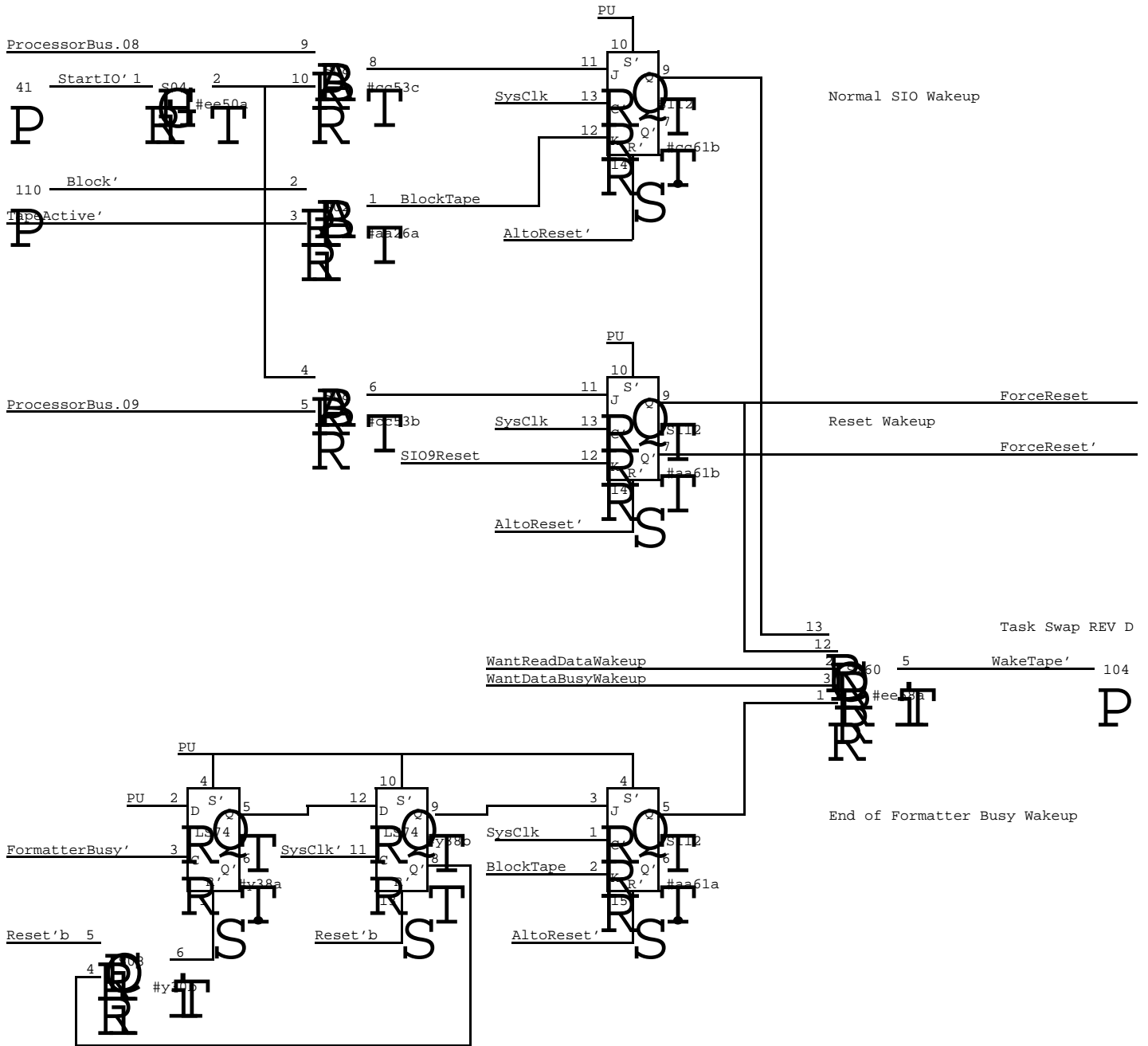


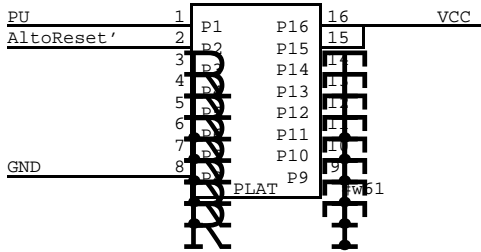
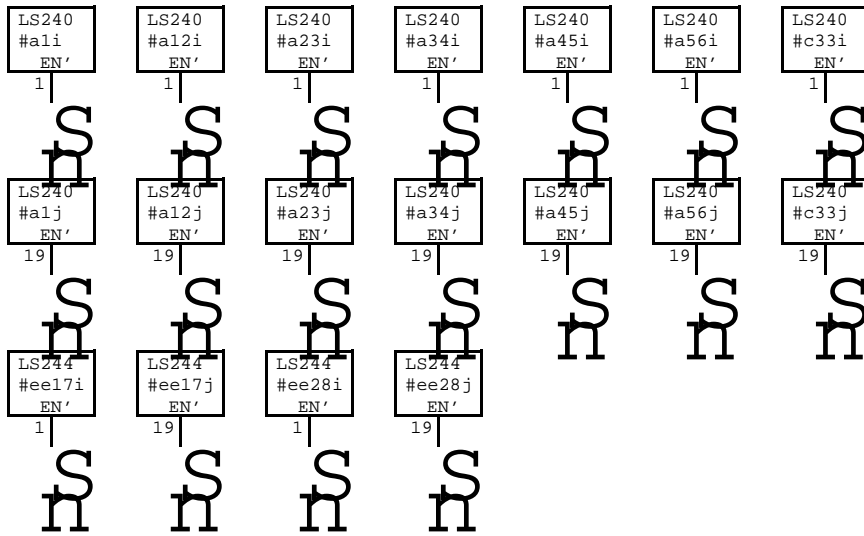
REV D



XEROX PARC/CSL	Project DDTape	Alto Processor Interface	File DDTape10.sil	Designer Tim Diebert	Rev D	Date 2/12/81	Page 11
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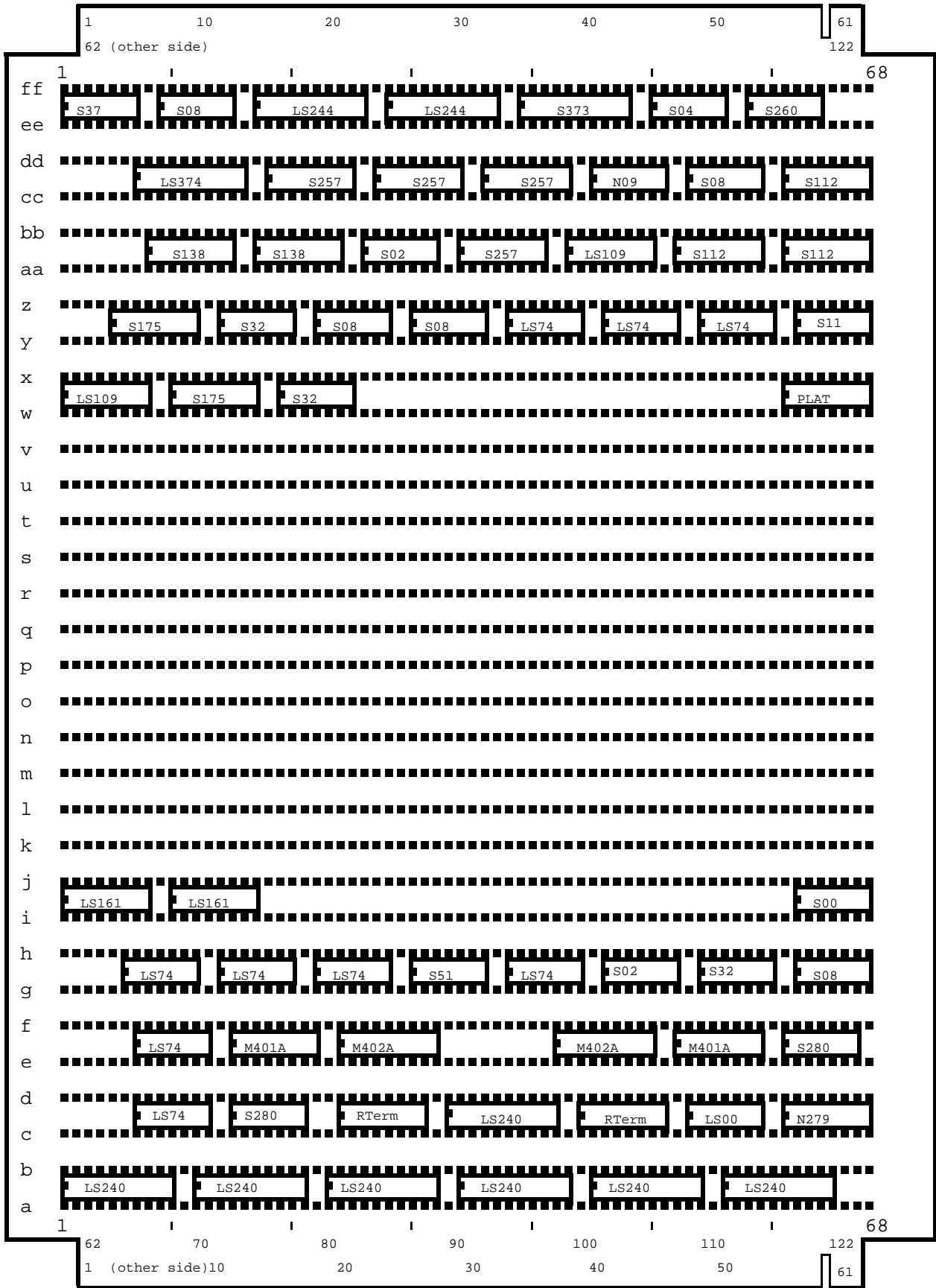






1k ohm resistor from 1 to 16
 330 ohm resistor from 2 to 15

E D G E C O N N E C T O R



C A B L E C O N N E C T O R

Misc Clean up REV D

As viewed from the component side

Load .01uf caps all available locations near chips
Install heavy ground connections from edge to power p.

XEROX PARC/CSL	Project DDTape	Reference Layout	File DDTape14.sil	Designer Tim Diebert	Rev D	Date 2/12/81	Page 15
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